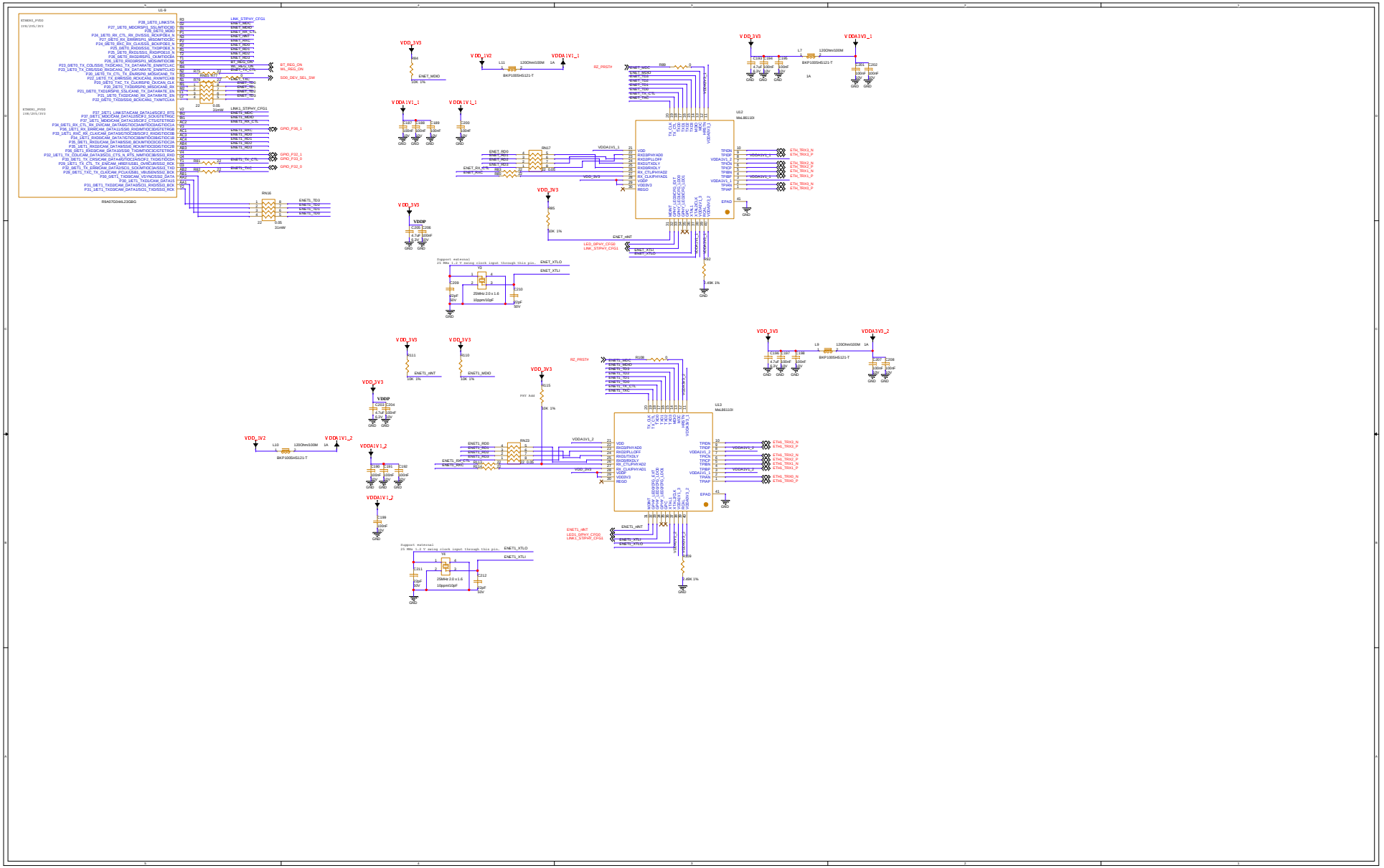
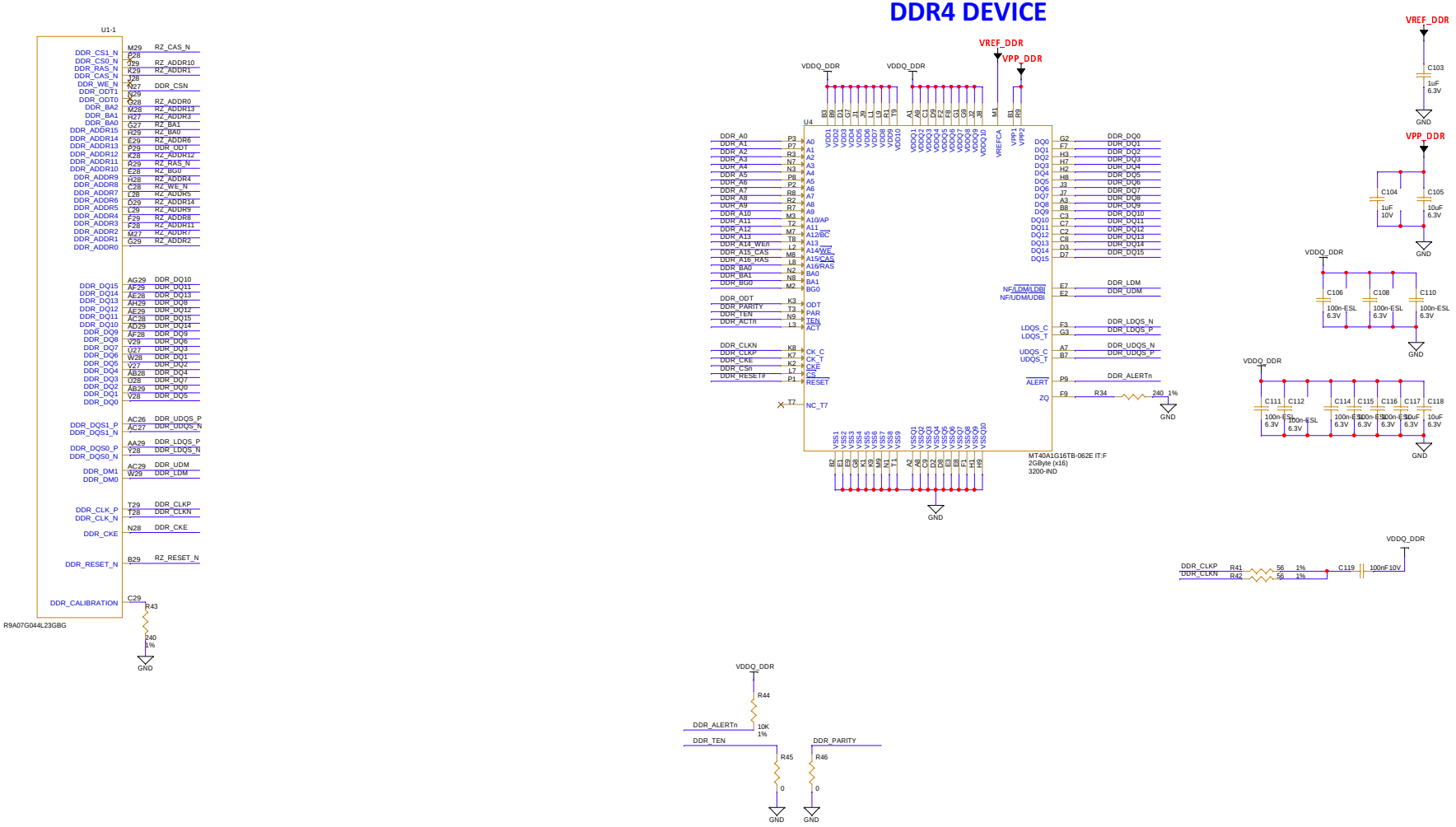


DDR4 DEVICE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DDR_CS0_N
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_ODT1
DDR_ODT0
DDR_BA2
DDR_BA1
DDR_BA0
DDR_ADDR15
DDR_ADDR14
DDR_ADDR13
DDR_ADDR12
DDR_ADDR11
DDR_ADDR10
DDR_ADDR9
DDR_ADDR8
DDR_ADDR7
DDR_ADDR6
DDR_ADDR5
DDR_ADDR4
DDR_ADDR3
DDR_ADDR2
DDR_ADDR1
DDR_ADDR0
RZ_CAS_N
RZ_ADDR10
RZ_ADDR1
DDR_CSN
RZ_ADDR0
RZ_ADDR13
RZ_ADDR3
RZ_BA1
RZ_BA0
RZ_ADDR6
DDR_ODT
RZ_ADDR12
RZ_RAS_N
RZ_BG0
RZ_ADDR4
RZ_WE_N
RZ_ADDR5
RZ_ADDR14
RZ_ADDR9
RZ_ADDR8
RZ_ADDR11
RZ_ADDR7
RZ_ADDR2
DDR_DQ15
DDR_DQ14
DDR_DQ13
DDR_DQ12
DDR_DQ11
DDR_DQ10
DDR_DQ9
DDR_DQ8
DDR_DQ7
DDR_DQ6
DDR_DQ5
DDR_DQ4
DDR_DQ3
DDR_DQ2
DDR_DQ1
DDR_DQ0
DDR_DQ10
DDR_DQ11
DDR_DQ13
DDR_DQ8
DDR_DQ12
DDR_DQ15
DDR_DQ14
DDR_DQ9
DDR_DQ6
DDR_DQ3
DDR_DQ1
DDR_DQ5
DDR_DQ7
DDR_DQ0
DDR_DQS1_P
DDR_DQS1_N
DDR_UDQS_P
DDR_UDQS_N
DDR_DQS0_P
DDR_DQS0_N
DDR_LDQS_P
DDR_LDQS_N
DDR_DM1
DDR_DM0
DDR_UDM
DDR_LDM
DDR_CLK_P
DDR_CLK_N
DDR_CLKP
DDR_CLKN
DDR_CKE
DDR_RESET_N
DDR_CALIBRATION
R43
240
1%
GND
U4
MT40A1G16TB-062E IT:F
2GByte (x16)
3200-IND
VDDQ_DDR
VREF_DDR
VPP_DDR
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_A14_WEn
DDR_A15_CAS
DDR_A16_RAS
DDR_BA0
DDR_BA1
DDR_BG0
DDR_ODT
DDR_PARITY
DDR_TEN
DDR_ACTn
DDR_CLKN
DDR_CLKP
DDR_CKE
DDR_CSn
DDR_RESET#
NC_T7
DDR_DQ0
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQ8
DDR_DQ9
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_LDM
DDR_UDM
DDR_LDQS_N
DDR_LDQS_P
DDR_UDQS_N
DDR_UDQS_P
DDR_ALERTn
R34
240
1%
C103
1uF
6.3V
C104
1uF
10V
C105
10uF
6.3V
C106
C108
C110
100n-ESL
6.3V
C111
C112
C114
C115
C116
C117
C118
10uF
6.3V
C119
100nF10V
R41
R42
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1%
R44
10K
1%
R45
R46
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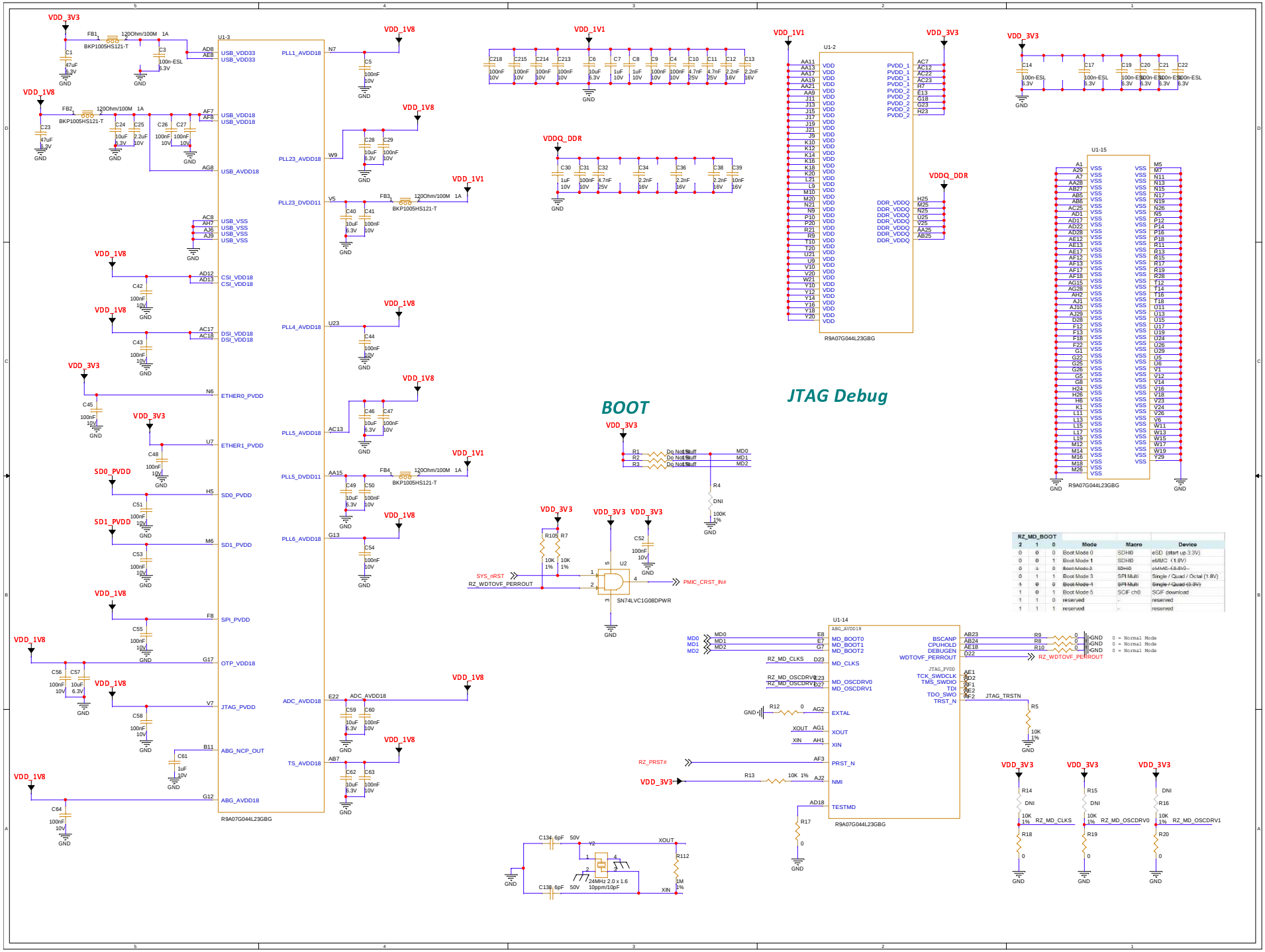

JTAG Debug
BOOT
R9A07G044L23GBG
SN74LVC1G08DPWR
RZ_MD_BOOT
2 1 0 Mode Macro Device
0 0 0 Boot Mode 0 SDHI0 eSD (start up 3.3V)
0 0 1 Boot Mode 1 SDHI0 eMMC (1.8V)
0 1 0 Boot Mode 2 SDHI0 eMMC (3.3V)
0 1 1 Boot Mode 3 SPI Multi Single / Quad / Octal (1.8V)
1 0 0 Boot Mode 4 SPI Multi Single / Quad (3.3V)
1 0 1 Boot Mode 5 SCIF ch0 SCIF download
1 1 0 reserved - reserved
1 1 1 reserved - reserved

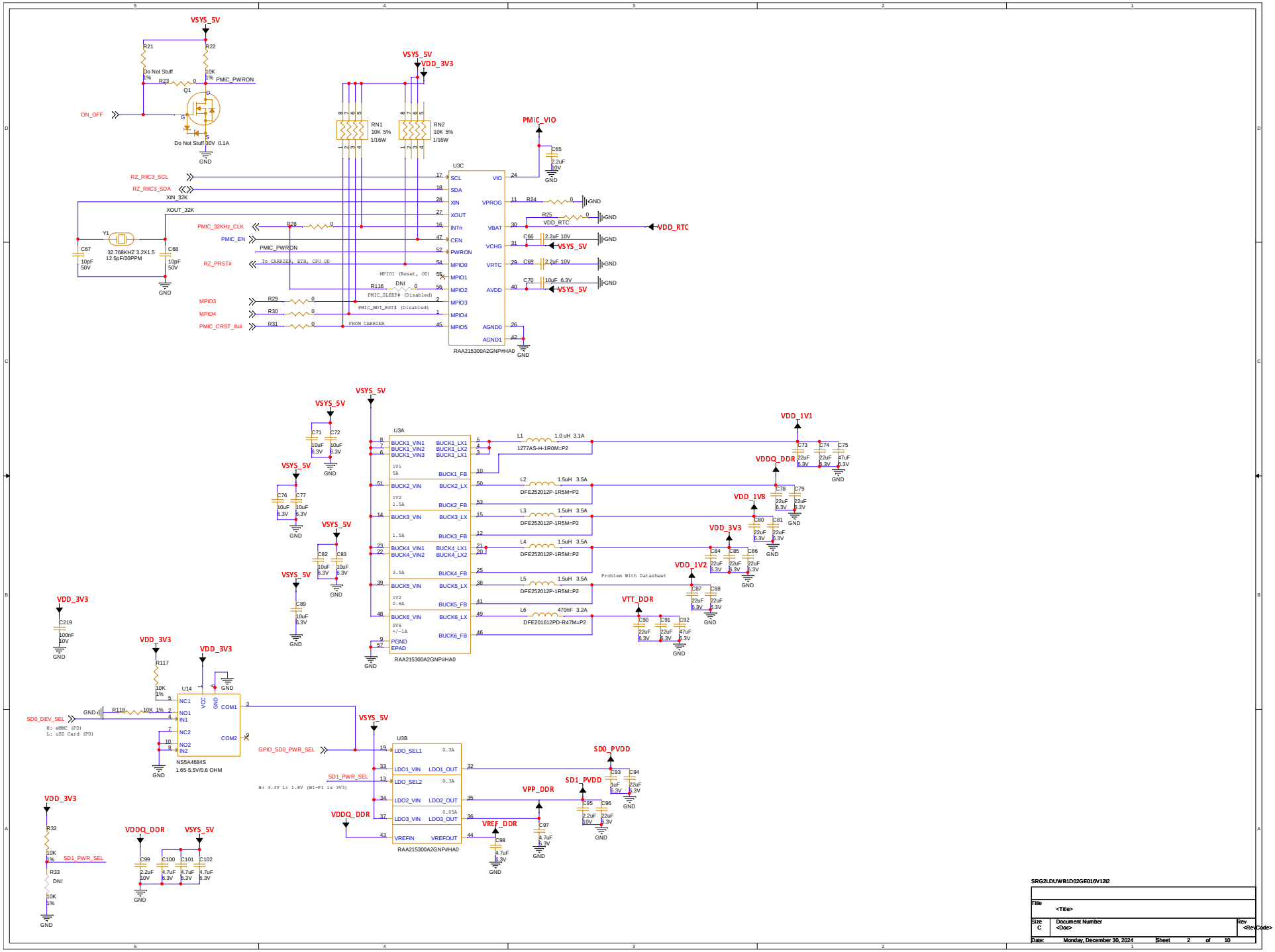
Table 1.1 Product Lineup

Group	Package	Part Number	CPU	Security*1
RZ/V2L	21 mm BGA	R9A07G054L28GBG	2× Cortex-A55, 1× Cortex-M33	Available
		R9A07G054L18GBG	1× Cortex-A55, 1× Cortex-M33	
		R9A07G054L24GBG	2× Cortex-A55, 1× Cortex-M33	Not supported
		R9A07G054L14GBG	1× Cortex-A55, 1× Cortex-M33	
	15 mm BGA	R9A07G054L27GBG	2× Cortex-A55, 1× Cortex-M33	Available
		R9A07G054L17GBG	1× Cortex-A55, 1× Cortex-M33	
		R9A07G054L23GBG	2× Cortex-A55, 1× Cortex-M33	Not supported
		R9A07G054L13GBG	1× Cortex-A55, 1× Cortex-M33	

Note 1 The product with security function supports the following features

Group	Package	Part Number	CPU	Security *
RZ/G2L	21mm BGA	R9A07G044L28GBG	2x Cortex-A55, 1x Cortex-M33	Available
		R9A07G044L18GBG	1x Cortex-A55, 1x Cortex-M33	
		R9A07G044L24GBG	2x Cortex-A55, 1x Cortex-M33	Not supported
		R9A07G044L14GBG	1x Cortex-A55, 1x Cortex-M33	
	15mm BGA	R9A07G044L27GBG	2x Cortex-A55, 1x Cortex-M33	Available
		R9A07G044L17GBG	1x Cortex-A55, 1x Cortex-M33	
		R9A07G044L23GBG	2x Cortex-A55, 1x Cortex-M33	Not supported
		R9A07G044L13GBG	1x Cortex-A55, 1x Cortex-M33	
RZ/G2LC	13mm BGA	R9A07G044C26GBG	2x Cortex-A55, 1x Cortex-M33	Available
		R9A07G044C16GBG	1x Cortex-A55, 1x Cortex-M33	
		R9A07G044C22GBG	2x Cortex-A55, 1x Cortex-M33	Not supported
		R9A07G044C12GBG	1x Cortex-A55, 1x Cortex-M33	

Note: * The product with security function supports the following features.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VDD_3V3
PMIC_VIO
VDD_RTC
VDDQ_DDR
VDD_1V8
VDD_1V1
VDD_1V2
VPP_DDR
VTT_DDR
VREF_DDR
SD0_PVDD
SD1_PVDD
U3C
RAA215300A2GNP#HA0
U3A
U3B
U14
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1.65-5.5V/0.6 OHM
Problem With Datasheet
SRG2LDUWB1D02GE016V12I2
Title
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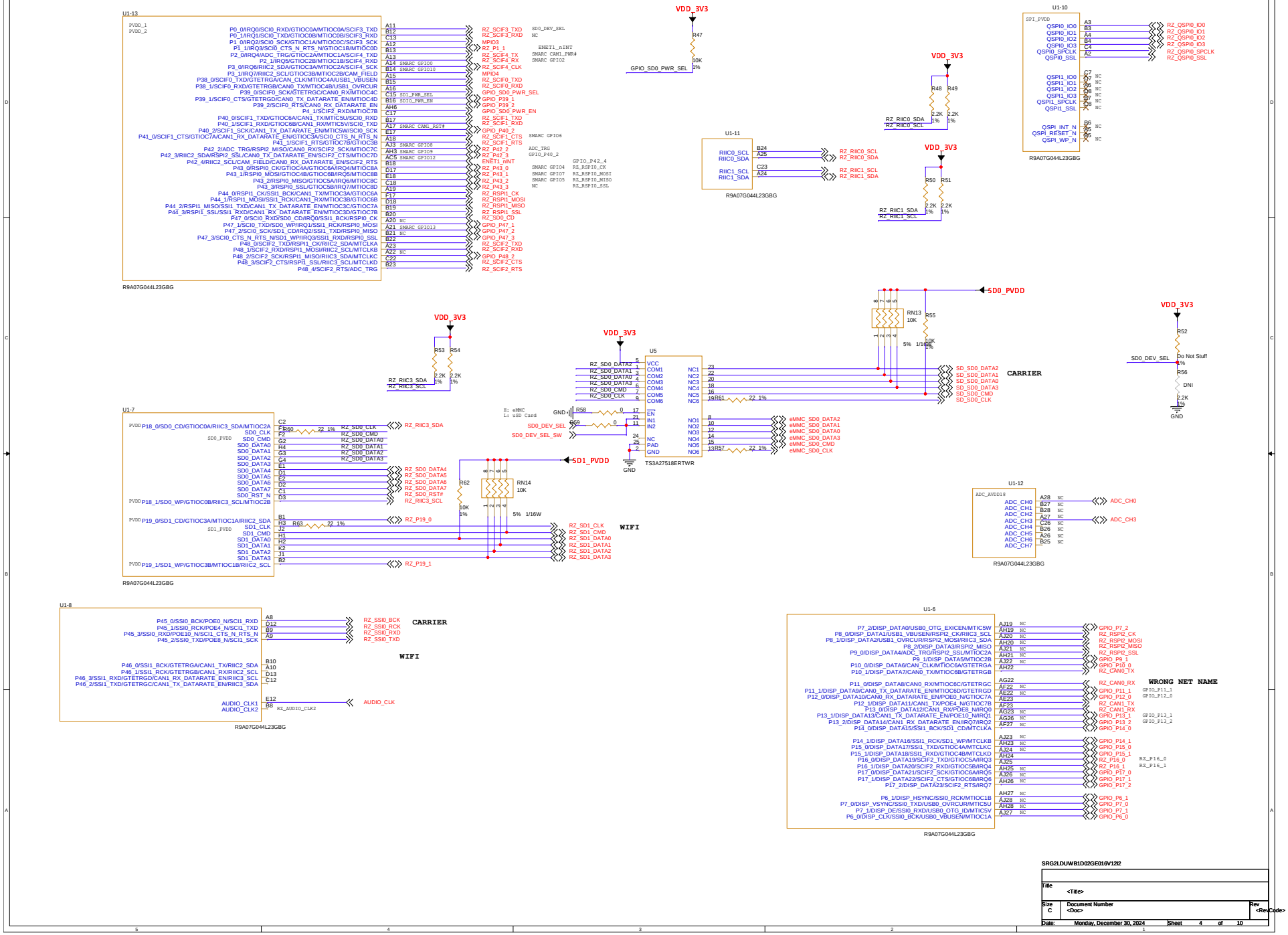
Size C
Document Number <Doc>
Rev <RevCode>
Date: Monday, December 30, 2024
Sheet 2 of 10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VDD_3V3
R47
10K
GPIO_SD0_PWR_SEL
U1-11
R9A07G044L23GBG
RZ_RIIC0_SDA
RZ_RIIC0_SCL
RZ_RIIC1_SDA
RZ_RIIC1_SCL
R48
R49
R50
R51
2.2K
U1-10
R9A07G044L23GBG
QSPI0_IO0
QSPI0_IO1
QSPI0_IO2
QSPI0_IO3
QSPI0_SPCLK
QSPI0_SSL
QSPI1_IO0
QSPI1_IO1
QSPI1_IO2
QSPI1_IO3
QSPI1_SPCLK
QSPI1_SSL
QSPI_INT_N
QSPI_RESET_N
QSPI_WP_N
SD0_PVDD
RN13
10K
R55
SD_SD0_DATA2
SD_SD0_DATA1
SD_SD0_DATA0
SD_SD0_DATA3
SD_SD0_CMD
SD_SD0_CLK
CARRIER
U5
TS3A27518ERTWR
RZ_SD0_DATA2
RZ_SD0_DATA1
RZ_SD0_DATA0
RZ_SD0_DATA3
RZ_SD0_CMD
RZ_SD0_CLK
VCC
COM1
COM2
COM3
COM4
COM5
COM6
NC1
NC2
NC3
NC4
NC5
NC6
EN
IN1
IN2
NO1
NO2
NO3
NO4
NO5
NO6
NC
PAD
GND
R58
R59
R61
R57
SD0_DEV_SEL
SD0_DEV_SEL_SW
H: eMMC
L: uSD Card
eMMC_SD0_DATA2
eMMC_SD0_DATA1
eMMC_SD0_DATA0
eMMC_SD0_DATA3
eMMC_SD0_CMD
eMMC_SD0_CLK
SD0_DEV_SEL
R52
Do Not Stuff
DNI
R56
U1-7
R9A07G044L23GBG
P18_0/SD0_CD/GTIOC0A/RIIC3_SDA/MTIOC2A
P18_1/SD0_WP/GTIOC0B/RIIC3_SCL/MTIOC2B
P19_0/SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA
P19_1/SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL
SD0_CLK
SD0_CMD
SD0_DATA0
SD0_DATA1
SD0_DATA2
SD0_DATA3
SD0_DATA4
SD0_DATA5
SD0_DATA6
SD0_DATA7
SD0_RST_N
SD1_CLK
SD1_CMD
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
RZ_RIIC3_SDA
RZ_RIIC3_SCL
RZ_P19_0
RZ_P19_1
RZ_SD0_RST#
RZ_SD1_CLK
RZ_SD1_CMD
RZ_SD1_DATA0
RZ_SD1_DATA1
RZ_SD1_DATA2
RZ_SD1_DATA3
WIFI
R53
R54
R60
R62
R63
RN14
10K
22
U1-12
R9A07G044L23GBG
ADC_AVDD18
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
U1-8
R9A07G044L23GBG
P45_0/SSI0_BCK/POE0_N/SCI1_RXD
P45_1/SSI0_RCK/POE4_N/SCI1_TXD
P45_3/SSI0_RXD/POE10_N/SCI1_CTS_N_RTS_N
P45_2/SSI0_TXD/POE8_N/SCI1_SCK
P46_0/SSI1_BCK/GTETRGA/CAN1_TX/RIIC2_SDA
P46_1/SSI1_RCK/GTETRGB/CAN1_RX/RIIC2_SCL
P46_3/SSI1_RXD/GTETRGD/CAN1_RX_DATARATE_EN/RIIC3_SCL
P46_2/SSI1_TXD/GTETRGC/CAN1_TX_DATARATE_EN/RIIC3_SDA
RZ_SSI0_BCK
RZ_SSI0_RCK
RZ_SSI0_RXD
RZ_SSI0_TXD
CARRIER
WIFI
AUDIO_CLK1
AUDIO_CLK2
RZ_AUDIO_CLK2
AUDIO_CLK
U1-6
R9A07G044L23GBG
P7_2/DISP_DATA0/USB0_OTG_EXICEN/MTIC5W
P8_0/DISP_DATA1/USB1_VBUSEN/RSPI2_CK/RIIC3_SCL
P8_1/DISP_DATA2/USB1_OVRCUR/RSPI2_MOSI/RIIC3_SDA
P8_2/DISP_DATA3/RSPI2_MISO
P9_0/DISP_DATA4/ADC_TRG/RSPI2_SSL/MTIOC2A
P9_1/DISP_DATA5/MTIOC2B
P10_0/DISP_DATA6/CAN_CLK/MTIOC6A/GTETRGA
P10_1/DISP_DATA7/CAN0_TX/MTIOC6B/GTETRGB
P11_0/DISP_DATA8/CAN0_RX/MTIOC6C/GTETRGC
P11_1/DISP_DATA9/CAN0_TX_DATARATE_EN/MTIOC6D/GTETRGD
P12_0/DISP_DATA10/CAN0_RX_DATARATE_EN/POE0_N/GTIOC7A
P12_1/DISP_DATA11/CAN1_TX/POE4_N/GTIOC7B
P13_0/DISP_DATA12/CAN1_RX/POE8_N/IRQ0
P13_1/DISP_DATA13/CAN1_TX_DATARATE_EN/POE10_N/IRQ1
P13_2/DISP_DATA14/CAN1_RX_DATARATE_EN/IRQ7/IRQ2
P14_0/DISP_DATA15/SSI1_BCK/SD1_CD/MTCLKA
P14_1/DISP_DATA16/SSI1_RCK/SD1_WP/MTCLKB
P15_0/DISP_DATA17/SSI1_TXD/GTIOC4A/MTCLKC
P15_1/DISP_DATA18/SSI1_RXD/GTIOC4B/MTCLKD
P16_0/DISP_DATA19/SCIF2_TXD/GTIOC5A/IRQ3
P16_1/DISP_DATA20/SCIF2_RXD/GTIOC5B/IRQ4
P17_0/DISP_DATA21/SCIF2_SCK/GTIOC6A/IRQ5
P17_1/DISP_DATA22/SCIF2_CTS/GTIOC6B/IRQ6
P17_2/DISP_DATA23/SCIF2_RTS/IRQ7
P6_1/DISP_HSYNC/SSI0_RCK/MTIOC1B
P7_0/DISP_VSYNC/SSI0_TXD/USB0_OVRCUR/MTIC5U
P7_1/DISP_DE/SSI0_RXD/USB0_OTG_ID/MTIC5V
P6_0/DISP_CLK/SSI0_BCK/USB0_VBUSEN/MTIOC1A
GPIO_P7_2
RZ_RSPI2_CK
RZ_RSPI2_MOSI
RZ_RSPI2_MISO
RZ_RSPI2_SSL
GPIO_P9_1
GPIO_P10_0
RZ_CAN0_TX
RZ_CAN0_RX
GPIO_P11_1
GPIO_P12_0
RZ_CAN1_TX
RZ_CAN1_RX
GPIO_P13_1
GPIO_P13_2
GPIO_P14_0
GPIO_P14_1
GPIO_P15_0
GPIO_P15_1
RZ_P16_0
RZ_P16_1
GPIO_P17_0
GPIO_P17_1
GPIO_P17_2
GPIO_P6_1
GPIO_P7_0
GPIO_P7_1
GPIO_P6_0
WRONG NET NAME
SRG2LDUWB1D02GE016V12I2
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Rev
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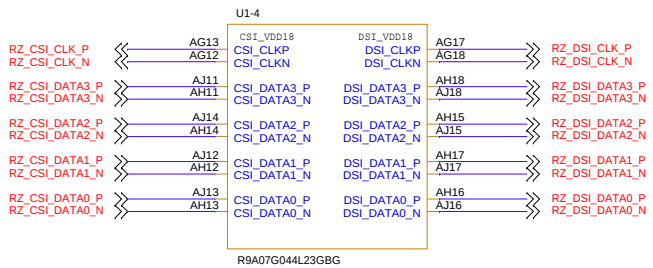
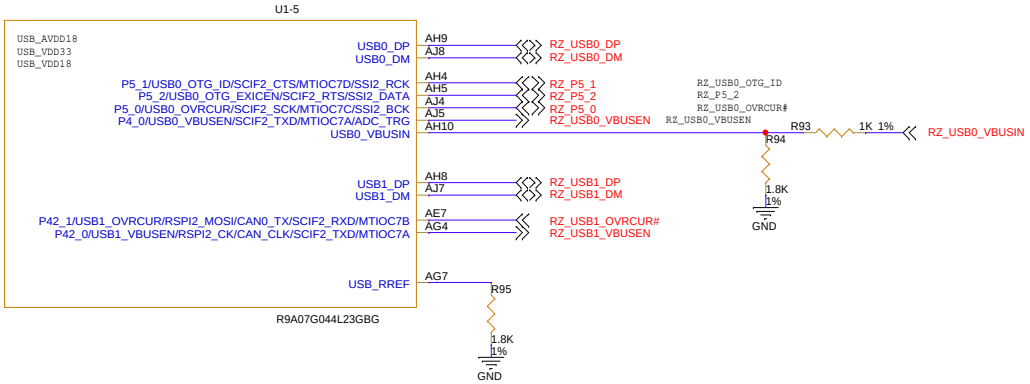
Date:
Monday, December 30, 2024
Sheet
4
of
10





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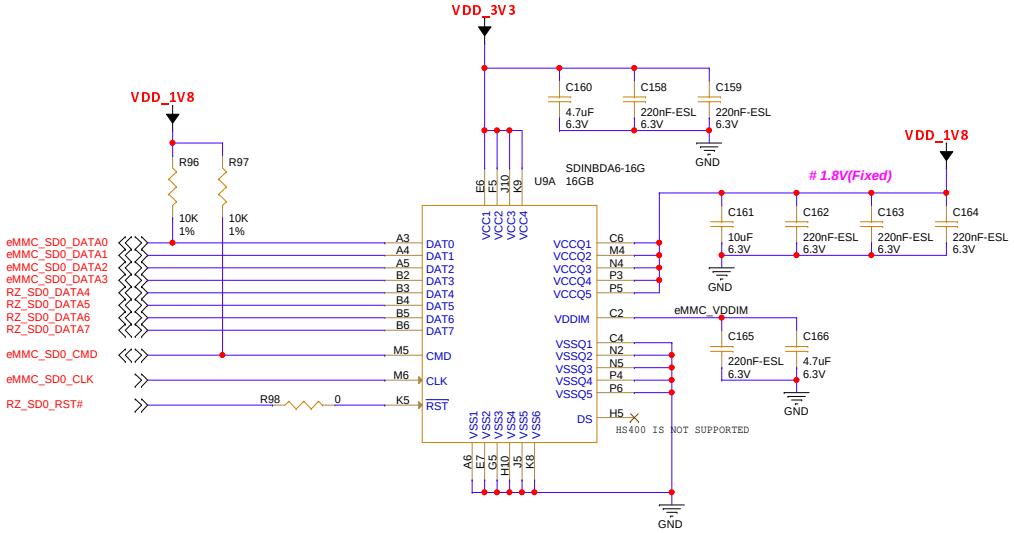
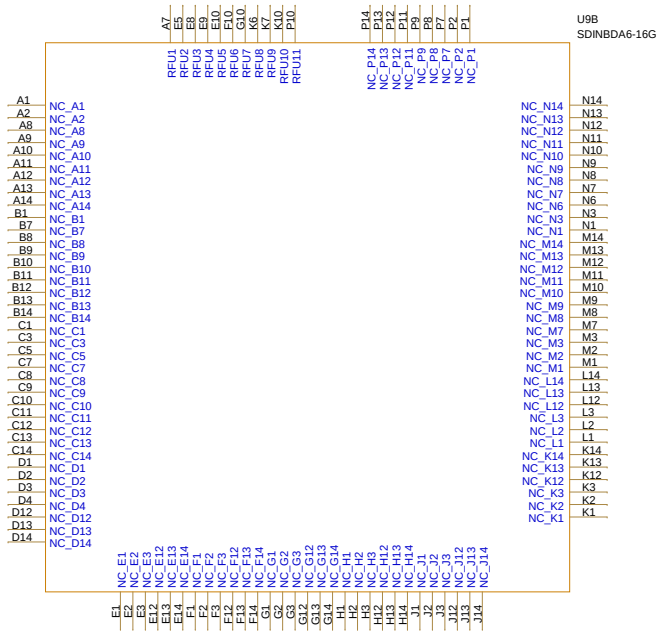
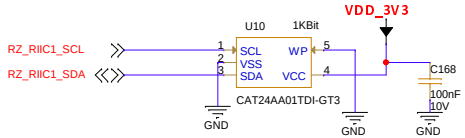
Date: Monday, December 30, 2024	Sheet 6 of 10	

Storage

eMMC5.1



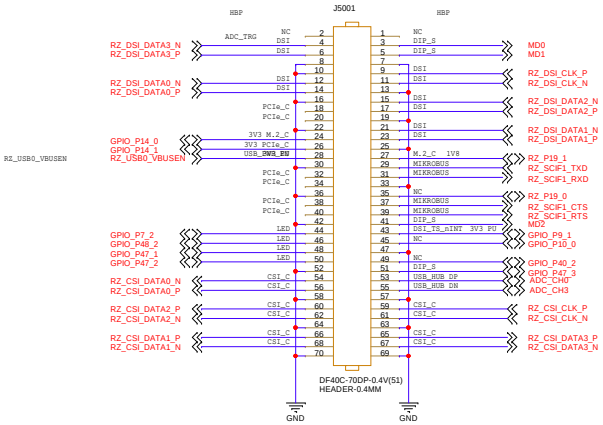


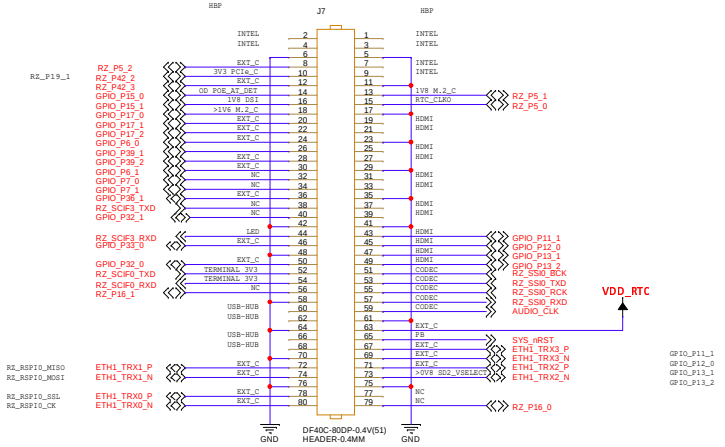


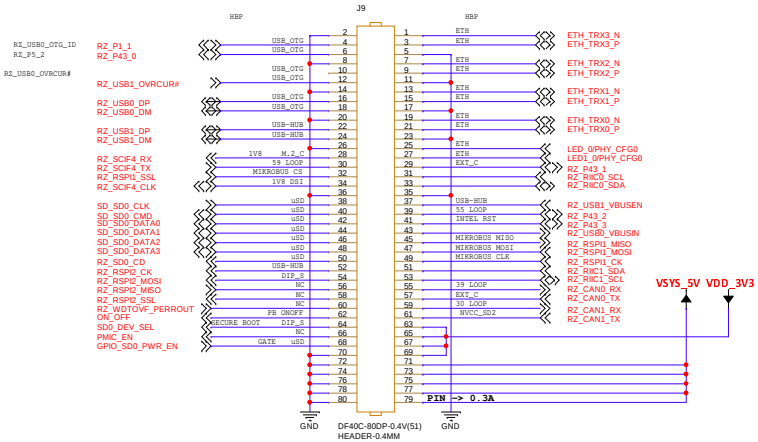
SRG2LDUWB1D02GE016V12I2

Size	Title	Rev
B	eMMC/EEPROM	1.1

Date: Monday, December 30, 2024 Sheet 7 of 10







SRG2LDUWB1D02GE016V12/2

Size	Title	Rev
C	B-T-B CONNECTORS	1.1
Date: Monday, December 30, 2024	Sheet 9 of 10	

Rev. 1.0	Prototype Version
Rev. 1.1 **Rev. 1.1.2**	1. Swapping between TX_CLK and TX_CTL in the Ethernet PHYs 2. Connecting ETH0 power to 3V3 3. Booting from carrier except Tutus
Rev. 1.2	1. Connect the WIFI clock (PMIC_32KHz_CLK) to Pull Up 2. Move RZ_P5_1 from J7-33 to J7-13 to support M.2 Reset on the HBP 3. Move RZ_P5_0 from J7-39 to J7-15 4. Move RZ_P5_2 from J7-37 to J7-8 5. Enable power control from BtB. Adding U14 (PU/PD select) 6. Move RZ_P16_0 from J7-59 to J7-79 7. Add AUDIO_CLK to J7-59 8. Add R116 to support RTC clock from MPIO2. 8. Swapping I2C1 pins on J9: J9-51-SDA, J9-53-SCL.

SRG2LDUWB1D02GE016V12I2

Size	Title	Rev
A	HISTORY	1.0

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