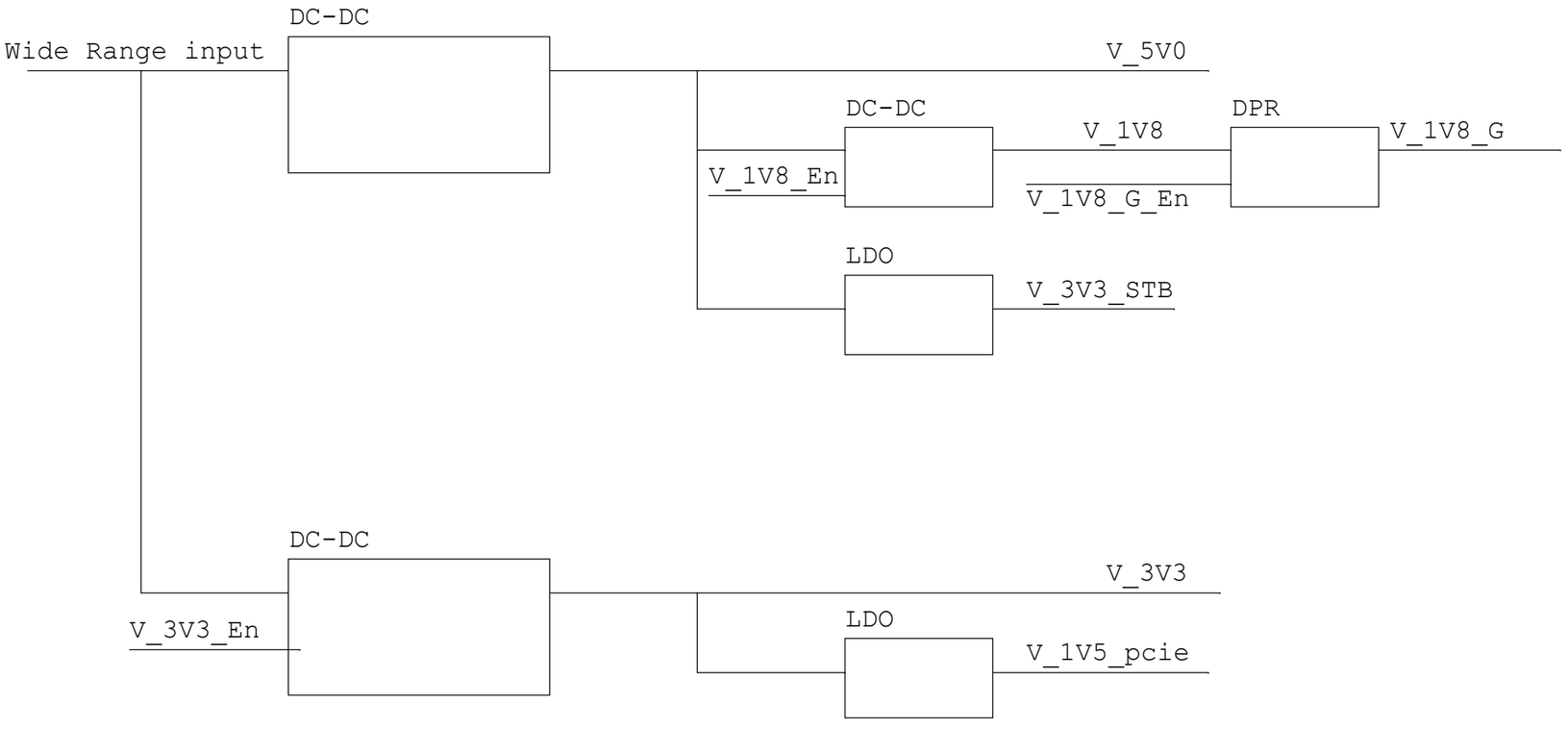
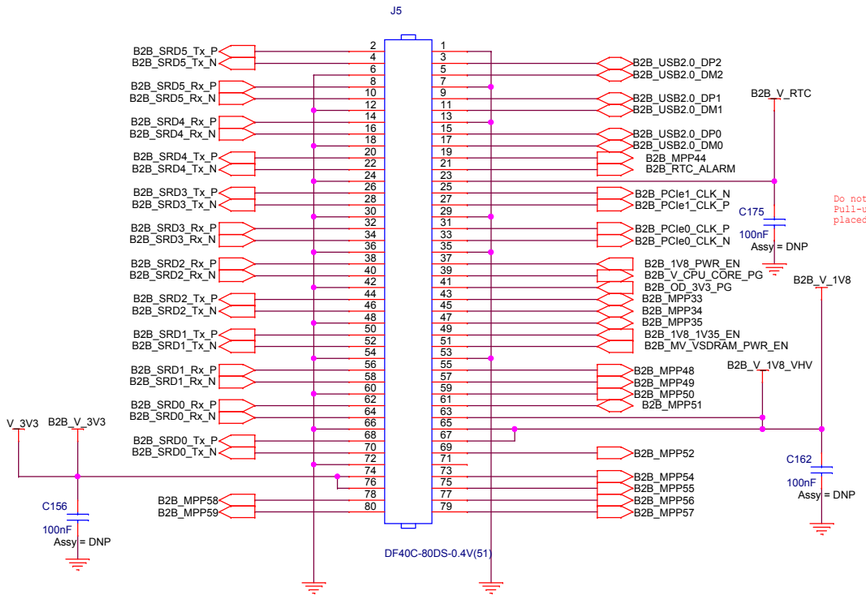
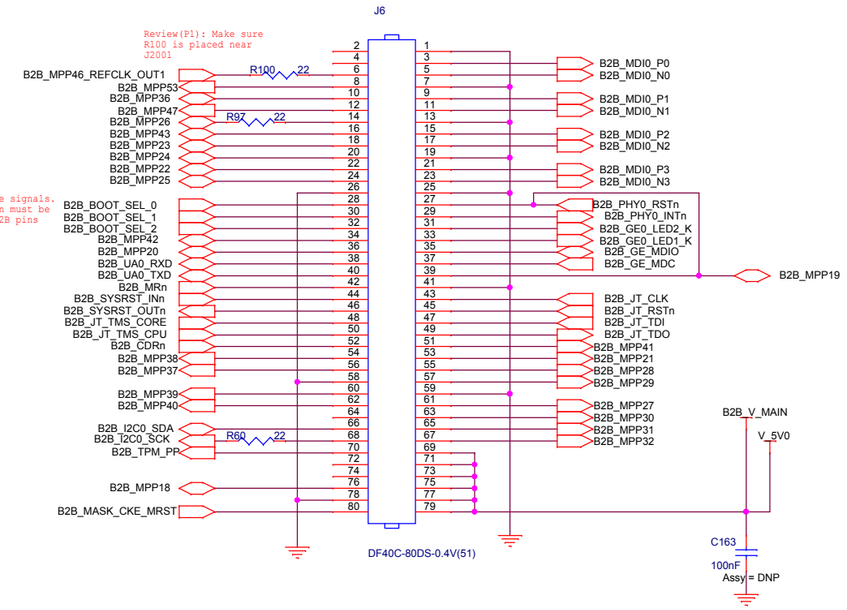
To Extract BOM:

Item\tQuantity\tAssemblyOption\tPart\tPCB Footprint\tDescription\tDataSheet\tManufacturer\tManufacturer P/N\tSolidRun P/N\tReference
{Item}\t{Quantity}\t{ASSY}\t{Value}\t{PCB Footprint}\t{DESCRIPTION}\t{Datasheet}\t{Manufacturer}\t{Manufacturer P/N}\t{SolidRun P/N}\t{Reference}

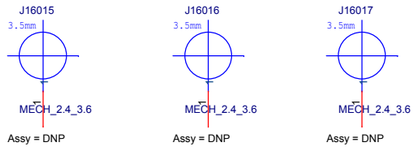


Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 1 of 19	





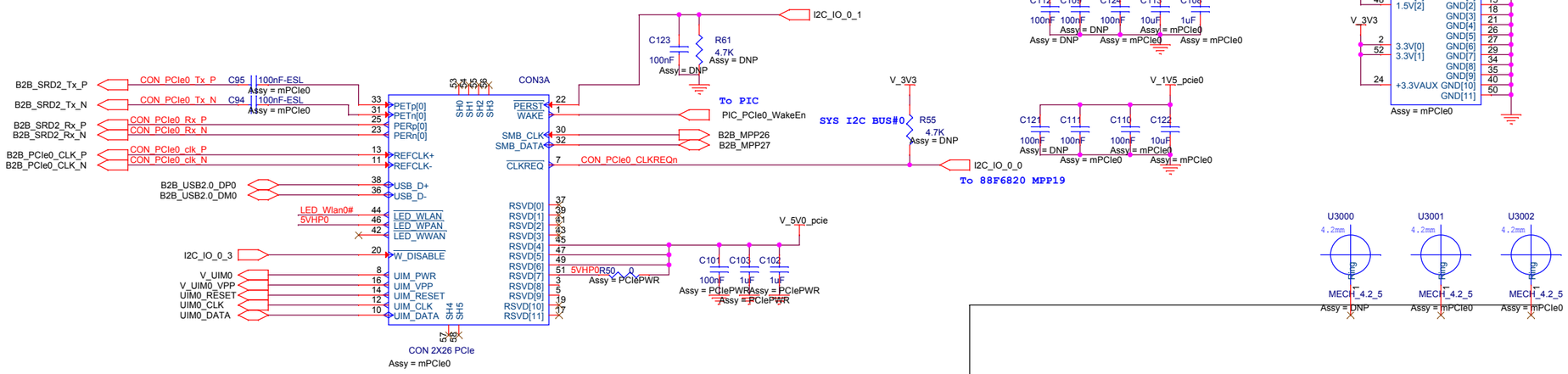
Three mechanical holes for the MicroSoM

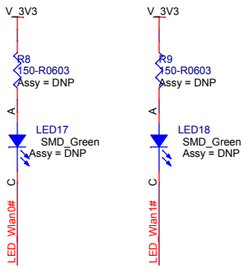


Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 2 of 19	

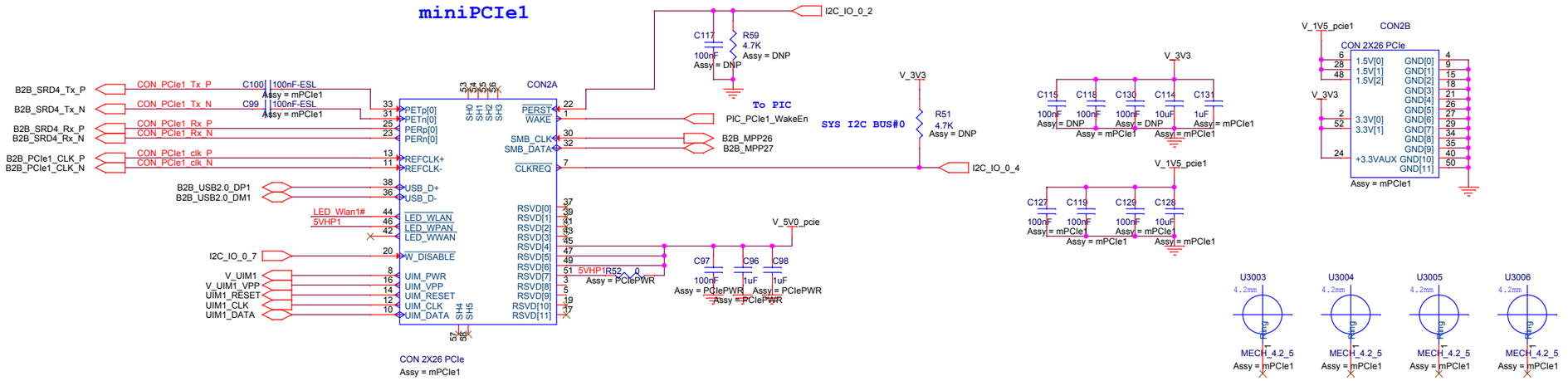
From 88F6820 SYSRST_OUT

miniPCIe0



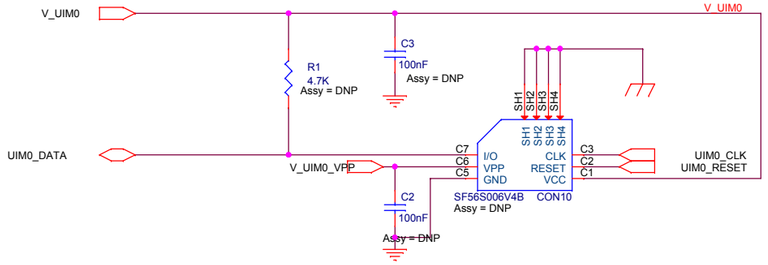


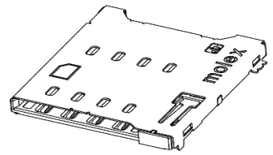
miniPCIe1



Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 3 of 19	

uSIM connector
Push-Push





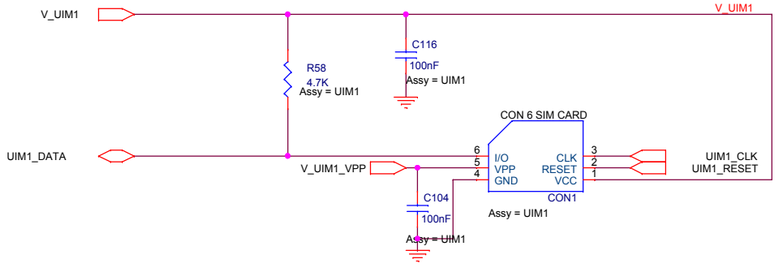
[SIM CARD PIN-MAP]

PIN NO.	DESCRIPTION
#1	Vcc(Supply V)
#2	RST(Reset)
#3	CLK(Clock)
#4	Reserved
#5	GND
#6	Vpp(Program V)
#7	I/O
#8	Reserved

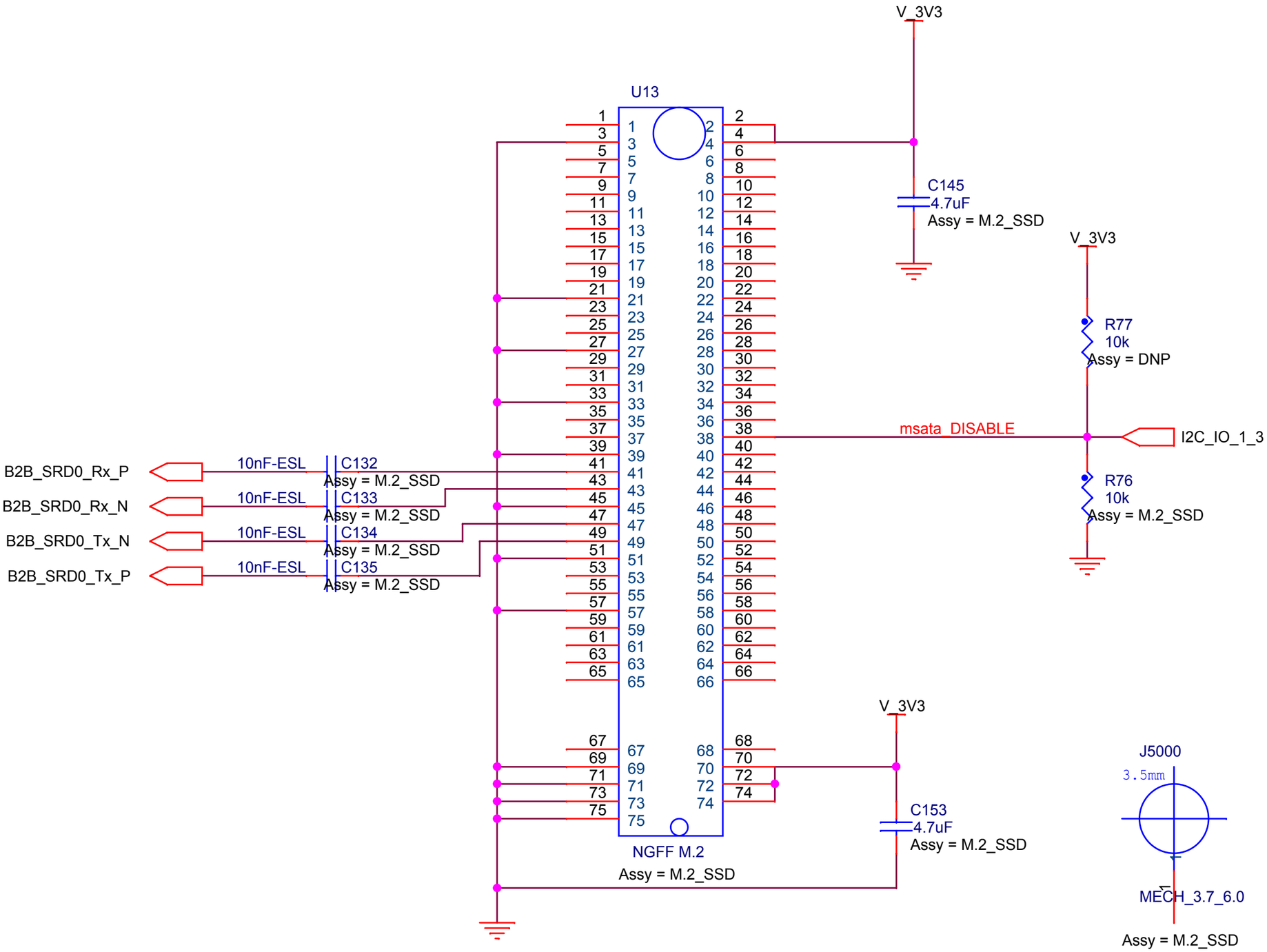
G1~G6	GND
Detect	Card Detector
Switch	Common/GND

Card Insertion Condition	DETECT SWITCH
Without Card	Open (OFF)
Card Insertion	Close (ON)

SIM connector
Henge



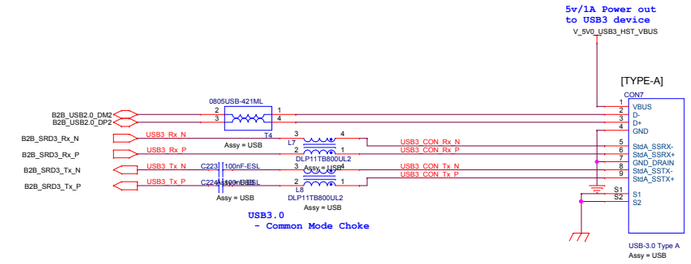
Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 4 of 19	



Size	Title	Rev
A	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 5 of 19	

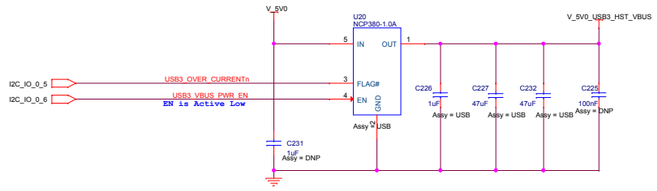
USB2.0
- Common Mode Choke

Connector side



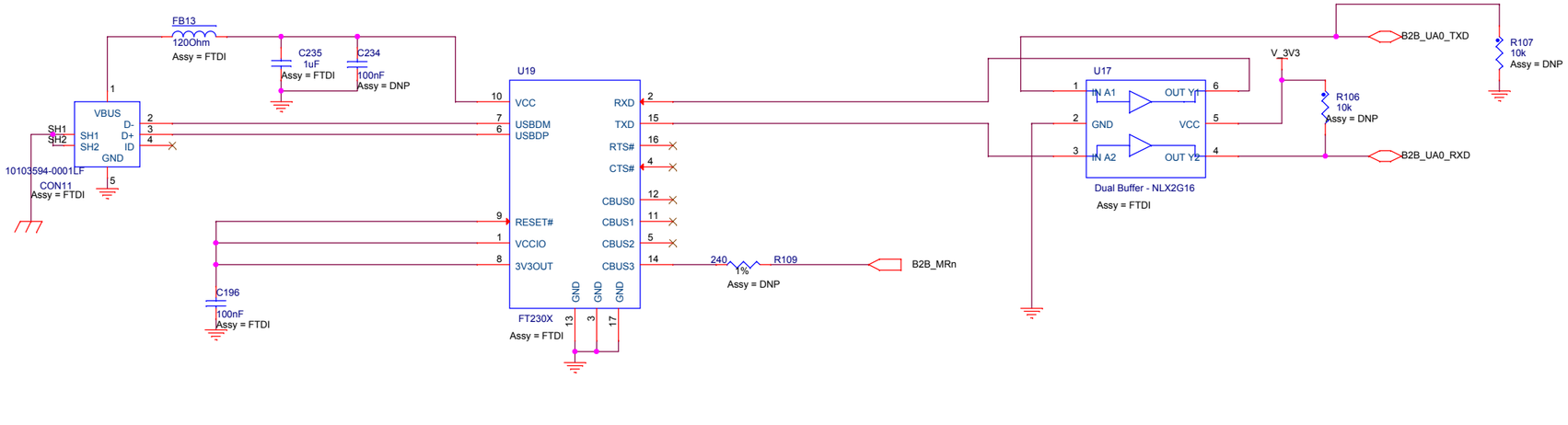
USB3.0
- Common Mode Choke

MV USB3.0 HOST



Size	Title	Rev
D	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 6 of 19	

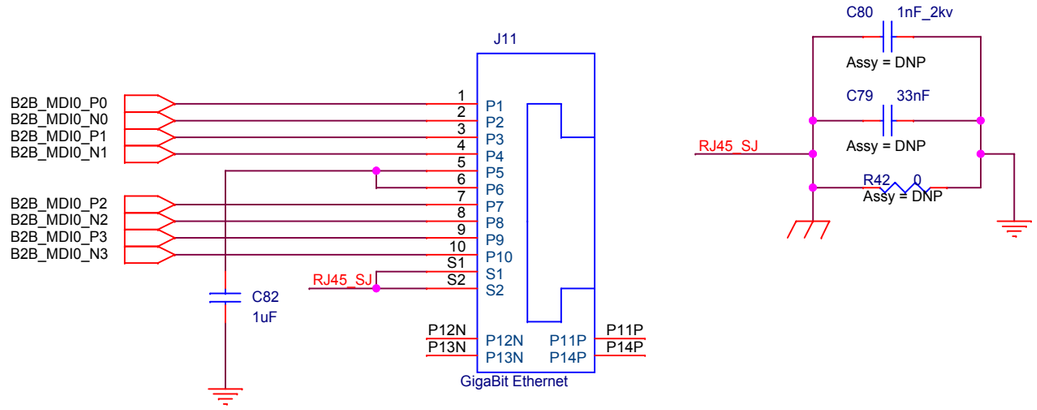
microUSB to UART

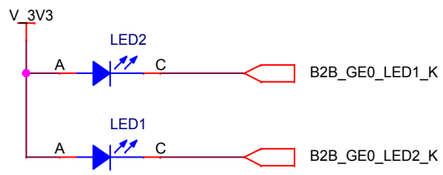


Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1

Date: Wednesday, October 28, 2015 Sheet 7 of 19

GE0: RJ45 Connector

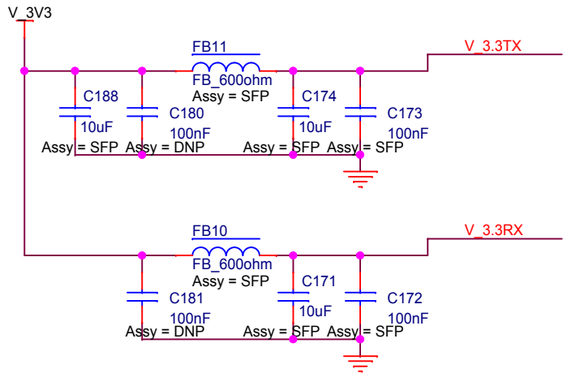


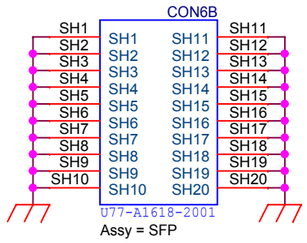


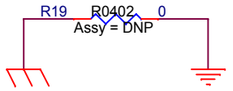
Size	Title	Rev
B	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 8 of 19	

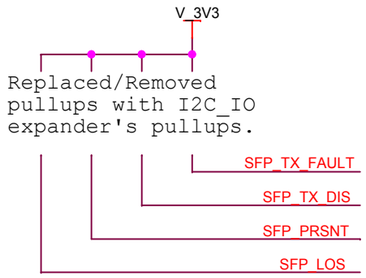
SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.

SFP TRANSCEIVER Power

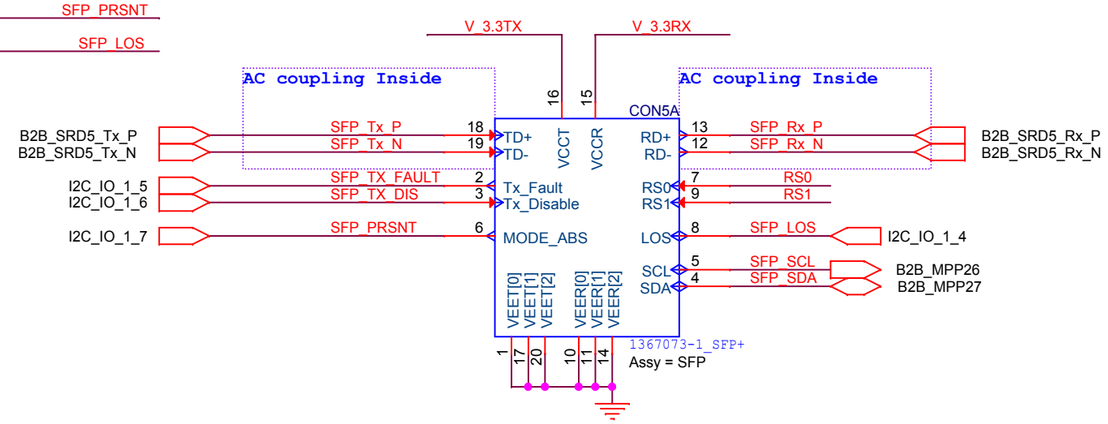


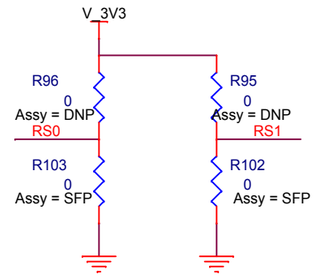






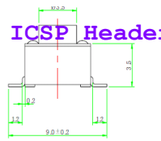
SFP TRANSCEIVER



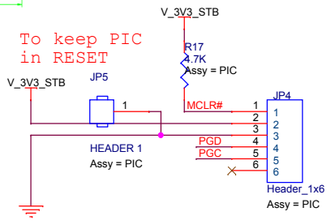


Size	Title	Rev
B	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 9 of 19	

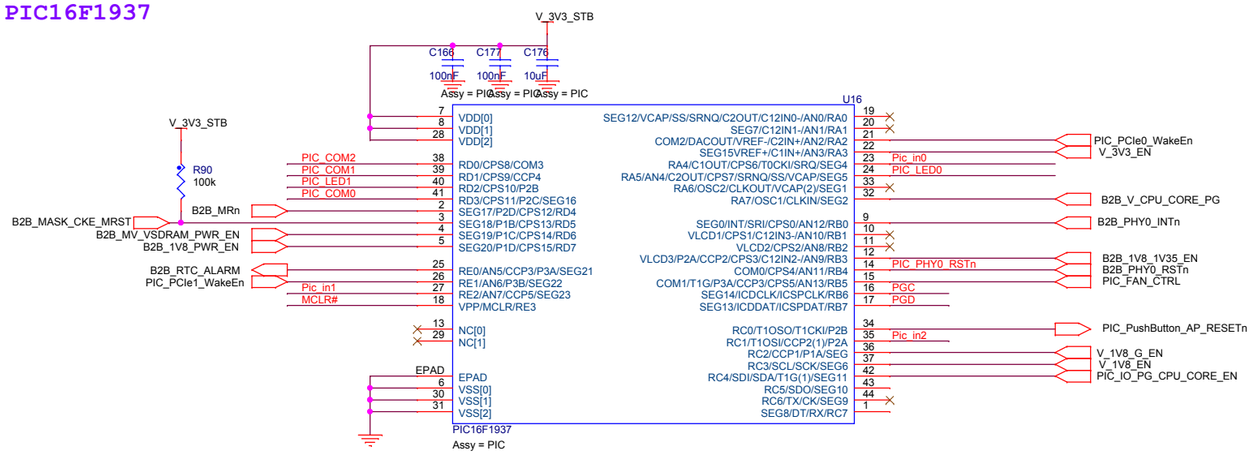
ICSP Header



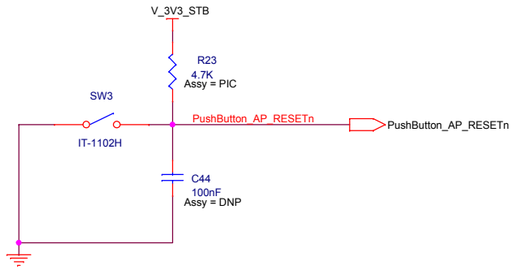
To keep PIC in RESET

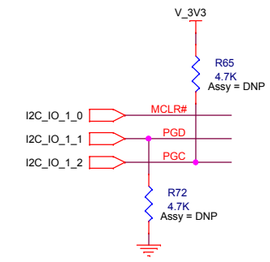


PIC16F1937

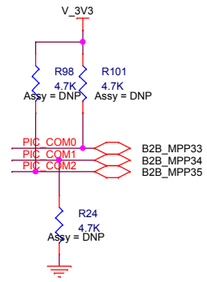


AP Reset Switch (GPIO)

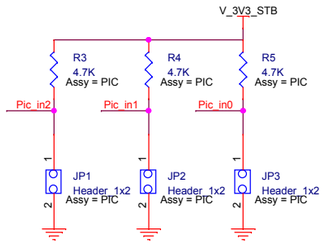




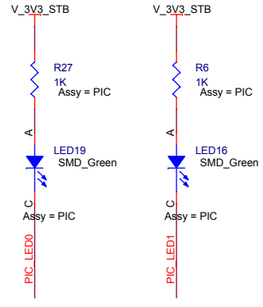
COM with MV Device



For SW Configuration Usage

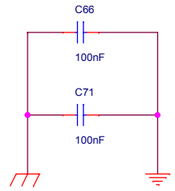


LEDs

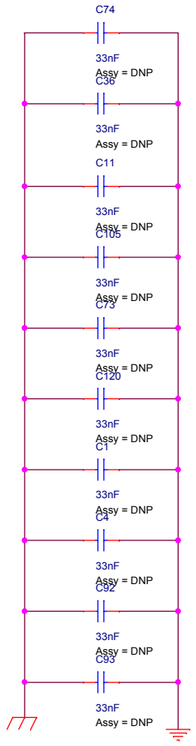


Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 10 of 19	

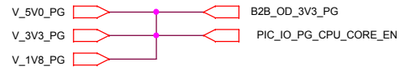
Bypass capacitors for MDIO
passing underneath GNDC

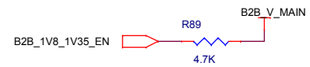


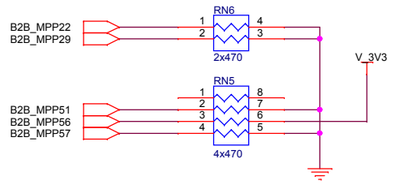
Bypass capacitors between GNDC and GND

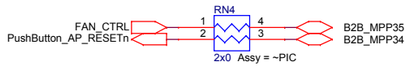


Carrier DC-DC PGOOD Signals will enable CPU DC-DC
on uSoM. Signal is pulled up on uSom.



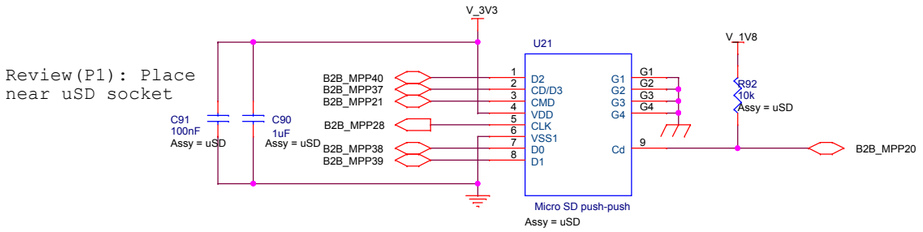




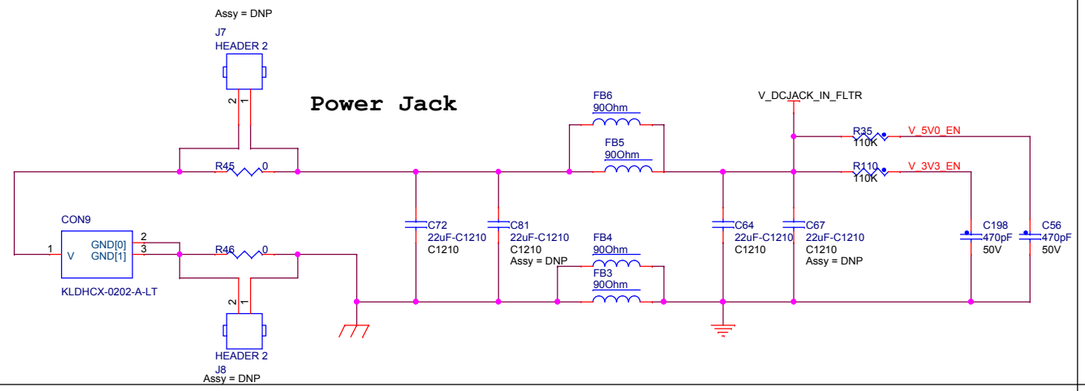


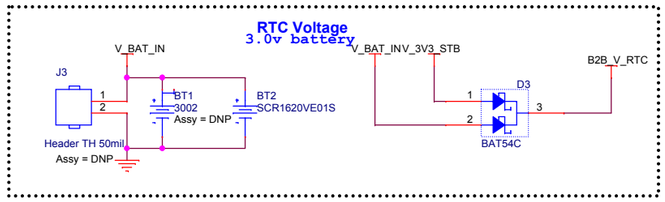
Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1*
Date: Wednesday, October 28, 2015	Sheet 11 of 19	

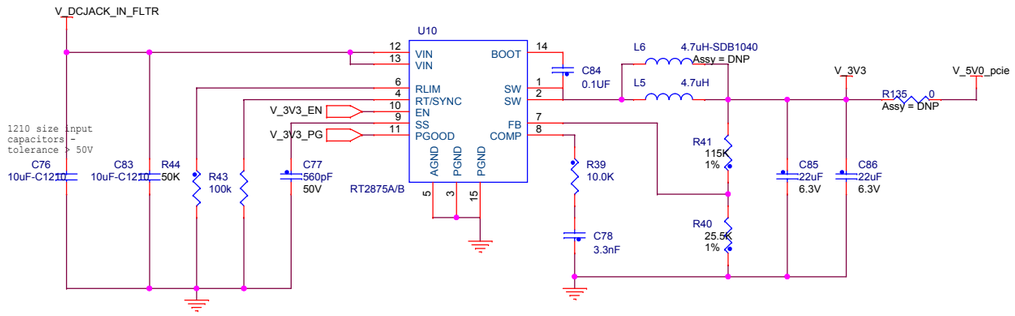
Review(P1): Place near uSD socket

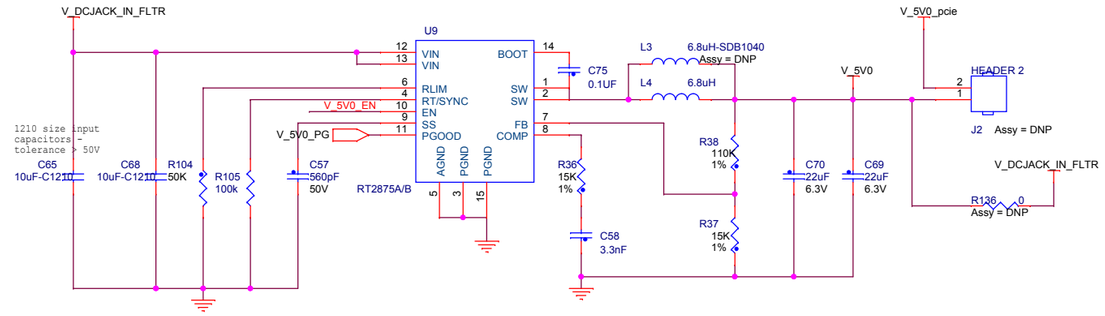


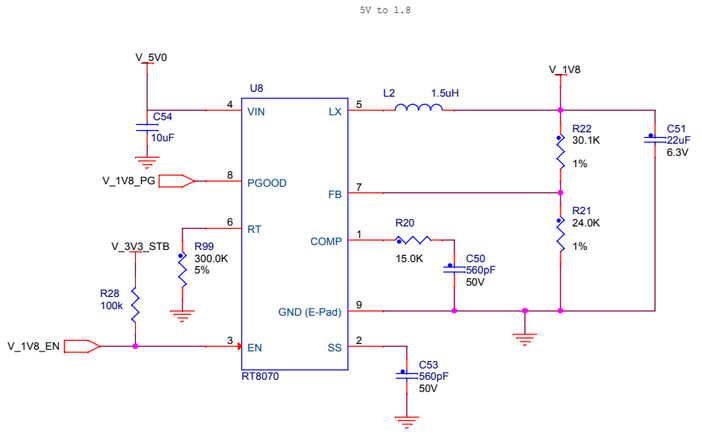
Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 12 of 19	

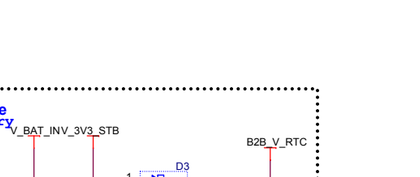




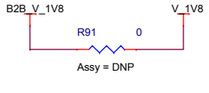


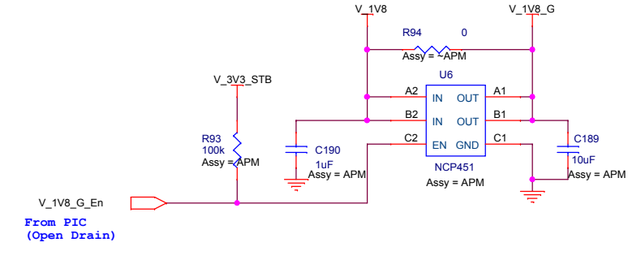






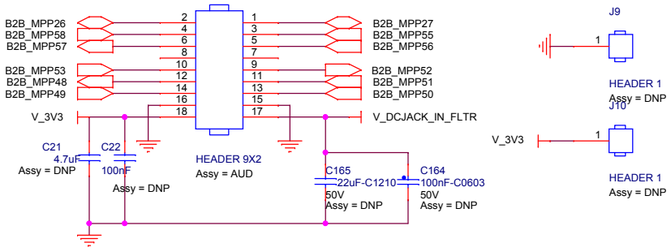
To be used if uSoM can power the carrier 1.8v domain.

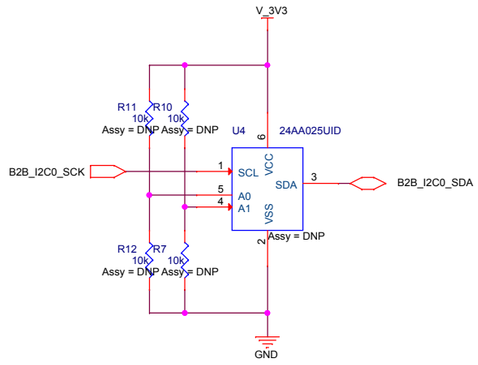


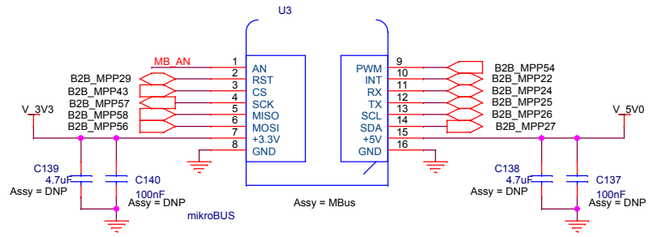


Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date:	Wednesday, October 28, 2015	Sheet 13 of 19

SLIC TDM Module connectors







PART NO.	XX	X	/XX
Device	Address Options	Temperature Range	Package

Device: MCP3021T: 10-Bit 2-Wire Serial A/D Converter (Tape and Reel)

Temperature Range: E = -40°C to +125°C

Address Options:

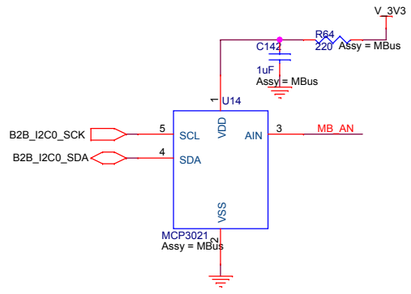
XX		A2	A1	A0
A0	=	0	0	0
A1	=	0	0	1
A2	=	0	1	0
A3	=	0	1	1
A4	=	1	0	0
A5 *	=	1	0	1
A6	=	1	1	0
A7	=	1	1	1

* Default option. Contact Microchip factory for other address options

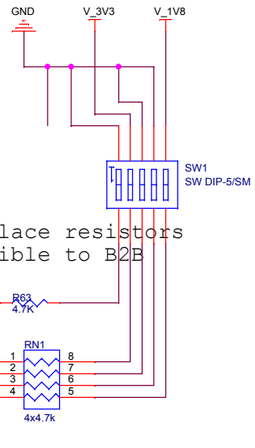
Package: OT = SOT-23, 5-lead (Tape and Reel)

Examples:

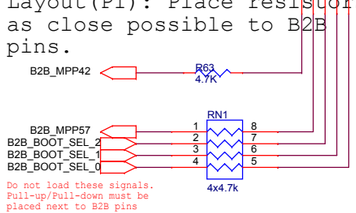
a) MCP3021A0T-E/OT: Extended, A0 Address, Tape and Reel
b) MCP3021A1T-E/OT: Extended, A1 Address, Tape and Reel
c) MCP3021A2T-E/OT: Extended, A2 Address, Tape and Reel
d) MCP3021A3T-E/OT: Extended, A3 Address, Tape and Reel
e) MCP3021A4T-E/OT: Extended, A4 Address, Tape and Reel
f) MCP3021A5T-E/OT: Extended, A5 Address, Tape and Reel
g) MCP3021A6T-E/OT: Extended, A6 Address, Tape and Reel
h) MCP3021A7T-IE/OT: Extended, A7 Address, Tape and Reel



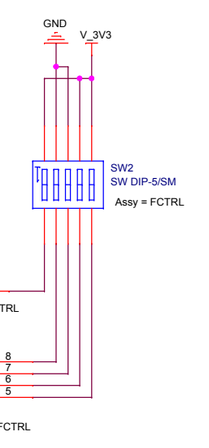
Internally pulled to 0x36:
110110

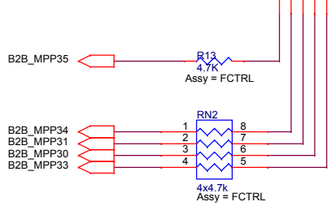


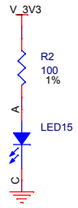
Layout(P1): Place resistors as close possible to B2B pins.



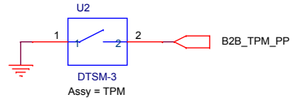
Internally pulled to 0x0c:
01100

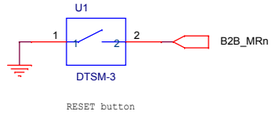




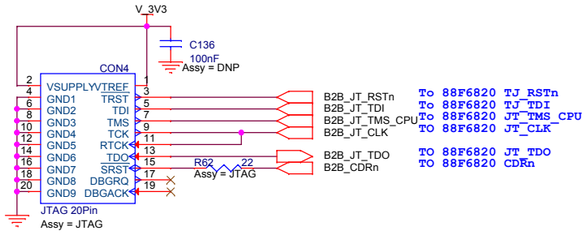


RESET button





RESET button



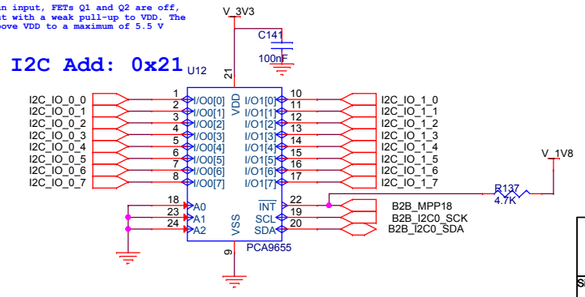
PCA9555
16-bit I2C and SMBus I/O port with interrupt
5 V tolerant I/Os

I/O port
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up to VDD. The input voltage may be raised above VDD to a maximum of 5.5 V

I/O Table

IO2_0
IO2_1
IO2_2
IO2_3
IO2_4
IO2_5
IO2_6
IO2_7
IO3_0
IO3_1
IO3_2
IO3_3
IO3_4
IO3_5
IO3_6
IO3_7

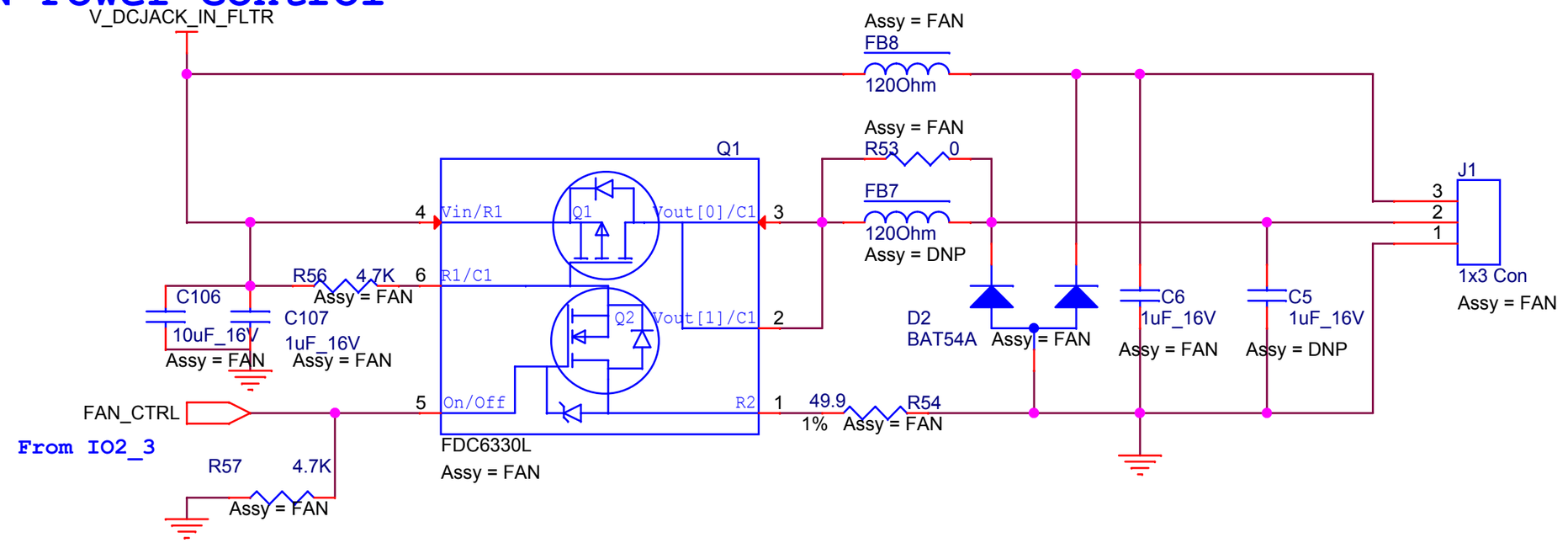
I2C Add: 0x21



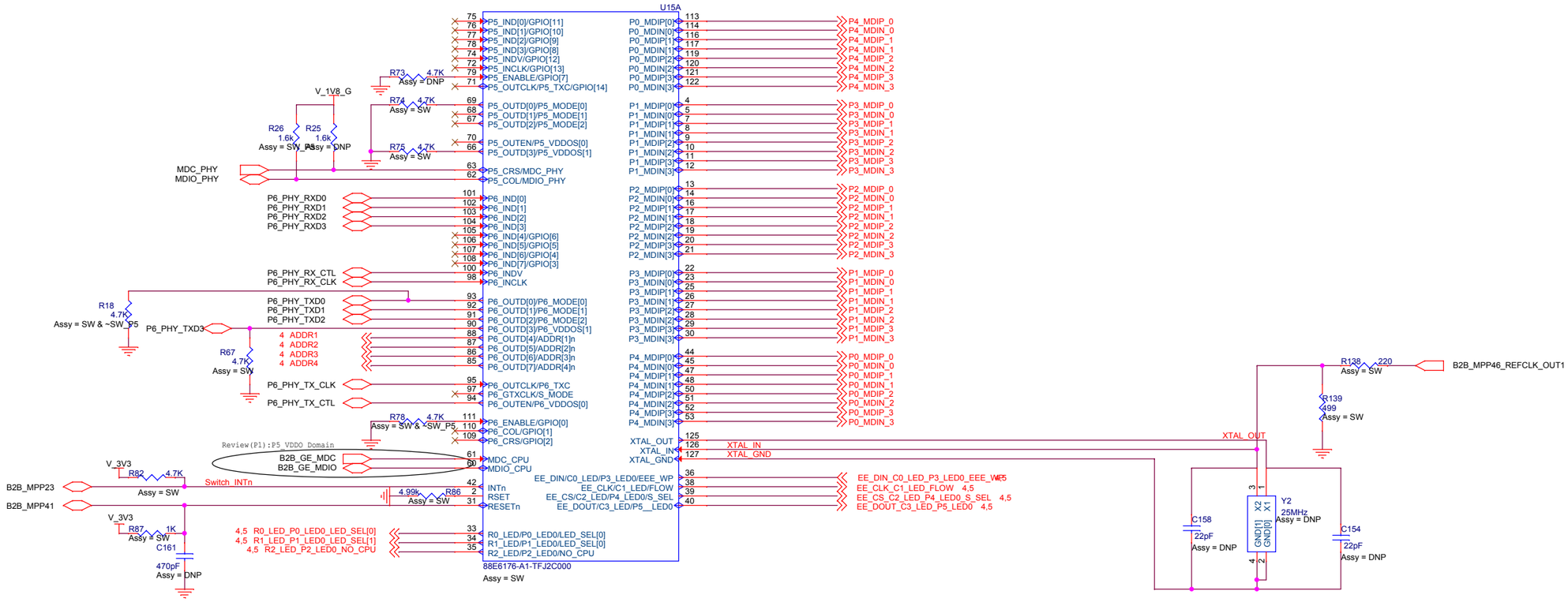
Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1

Date: Wednesday, October 28, 2015 Sheet 14 of 19

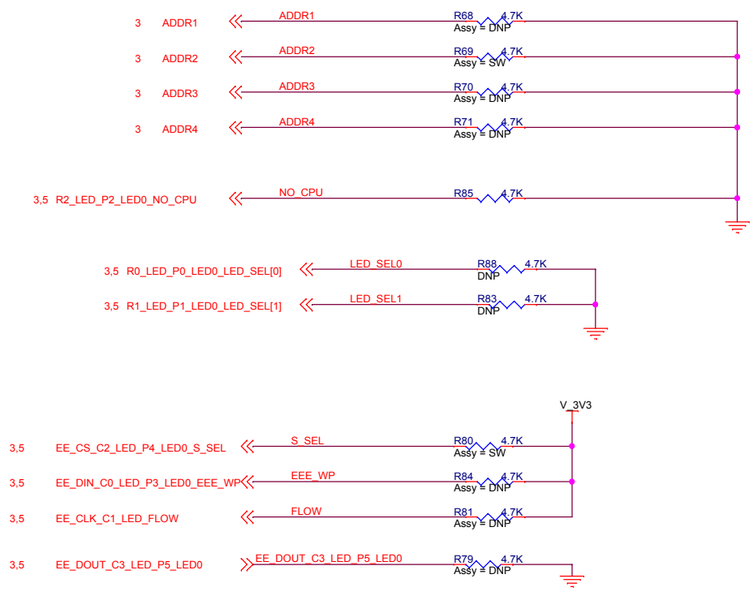
FAN Power Control



Size	Title	Rev
A	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 15 of 19	



ADDR0 = alway 0x0
SMI ADDRESS is the inverted value = 0x4

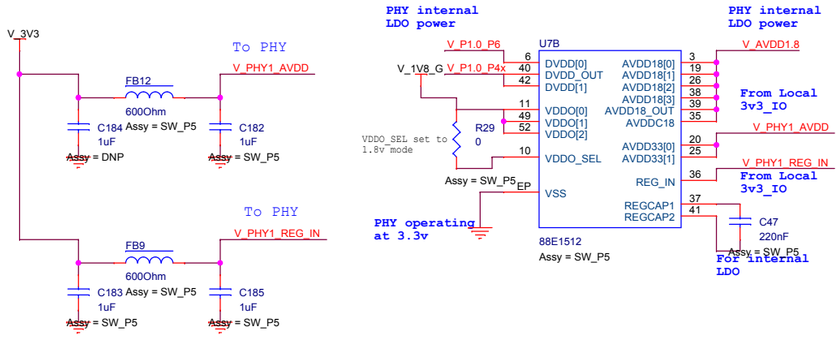


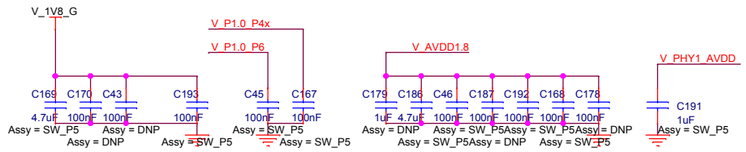
Pin	Name	Functionality	Default	Jumper/ DPR
35	NO_CPU	CPU ATTACHED	PU	PD.NC
34	LED_SEL[1]	LED Functionality	PU	PD.NC
33	LED_SEL[0]	LED Functionality	PU	PD.NC
39	S_SEL	Connect serdes to port 4 or 5	PD	PU
38	FLOW	Advertise auto-neg flow control	PD	PU
36	EEE_WP	Enable energy efficient Ethernet	PD	PU.NC
70	P5_VDDOS[0]	Port 5 power rail select	PU	PD
66	P5_VDDOS[1]	Port 5 power rail select	PU	PU
67,68,69	P5_OUTD[2:0]	0x7 = RGMII	PU	No option
94	P6_VDDOS[0]	Port 6 power rail select	PU	PD
90	P6_VDDOS[1]	Port 6 power rail select	PU	PU
91,92,93	P6_OUTD[2:0]	0x7 = RGMII	PU	No option
85,86,87,88	ADDR[4:1]n	SMI ADDRESS	PU	0x2

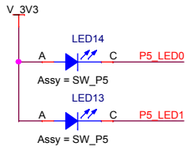
Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1
Date: Wednesday, October 28, 2015	Sheet 16 of 19	

PHY Power configurations

88E1512 power configurations:
1. using internal 1v8 and 1v0 regulators.
2. VDDO_SEL configs VDDO to operate at 2v5/3v3.







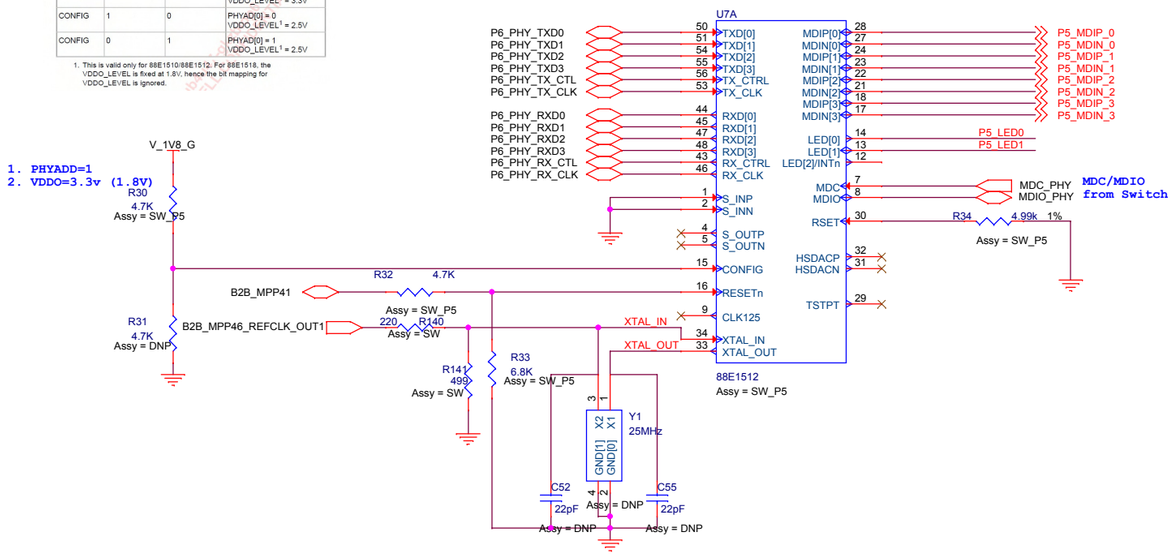
PHYADD configuration

88E1512 PHY configuration options:
PHY_address=1

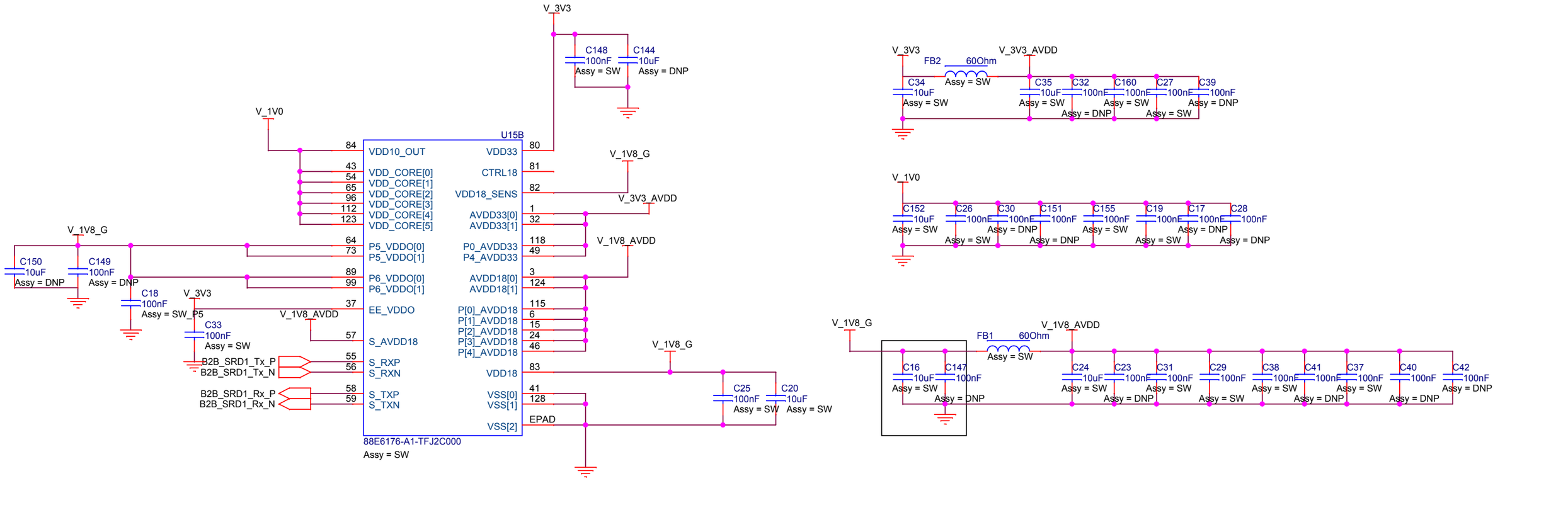
Table 53: Configuration Mapping

Pin	CONFIG Bit1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYAD[0] = 0 VDDO_LEVEL[1] = 3.3V
CONFIG	1	1	PHYAD[0] = 1 VDDO_LEVEL[1] = 3.3V
CONFIG	1	0	PHYAD[0] = 0 VDDO_LEVEL[1] = 2.5V
CONFIG	0	1	PHYAD[0] = 1 VDDO_LEVEL[1] = 2.5V

1. This is valid only for 88E1510/88E1512. For 88E1518, the VDDO_LEVEL is fixed at 1.8V, hence the bit mapping for VDDO_LEVEL is ignored.



Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1*
Date: Wednesday, October 28, 2015	Sheet 17 of 19	

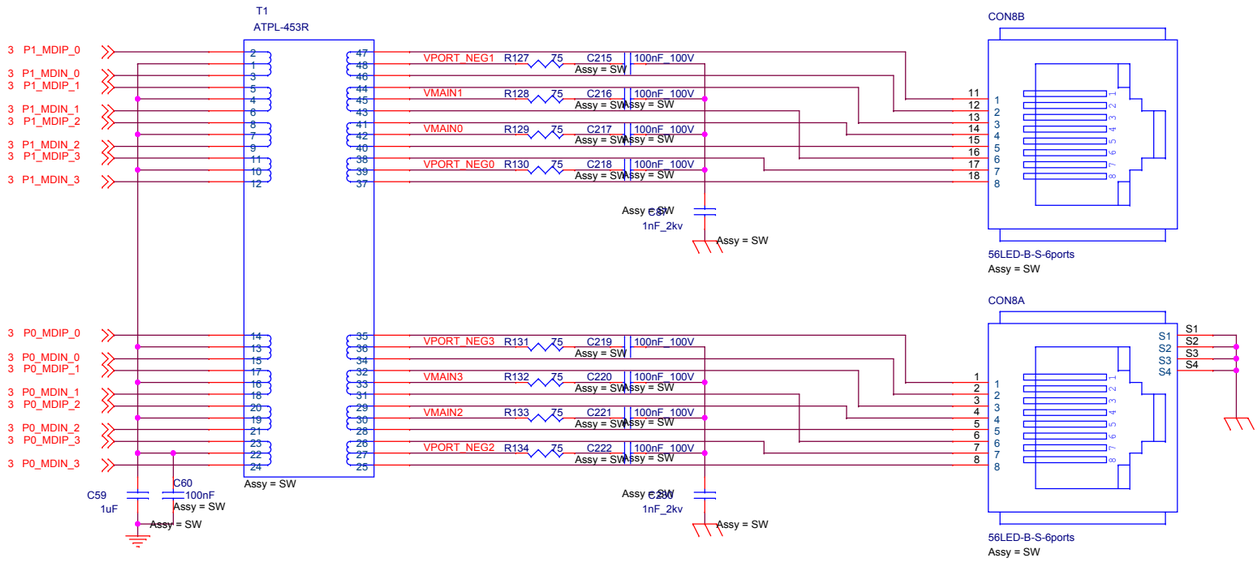


Size	Title	Rev
B	ClearFog Pro Evaluation Board	Rev-2.1

Date: Wednesday, October 28, 2015 Sheet 18 of 19

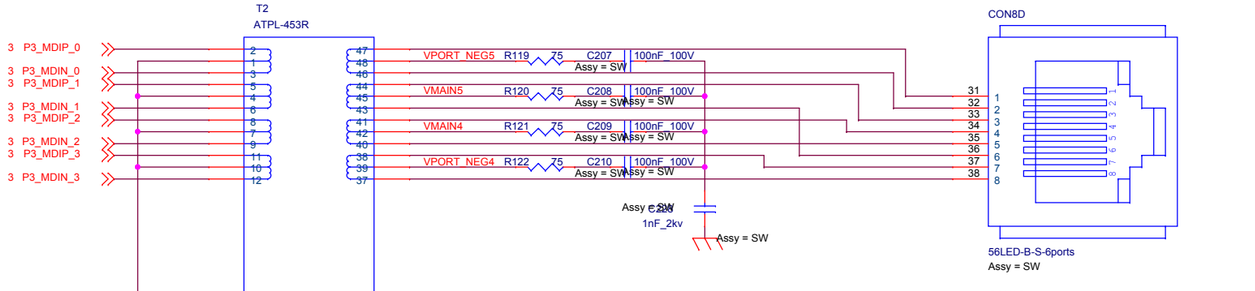
PoE Module connector, including two mechanical pins

PORT-1 MDI I/F

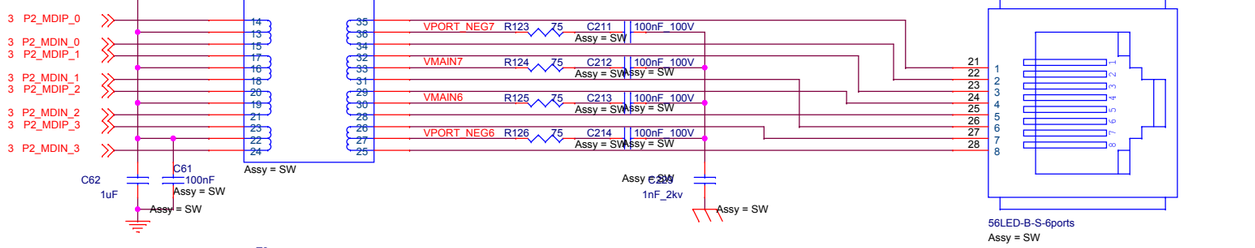


PORT-0 MDI I/F

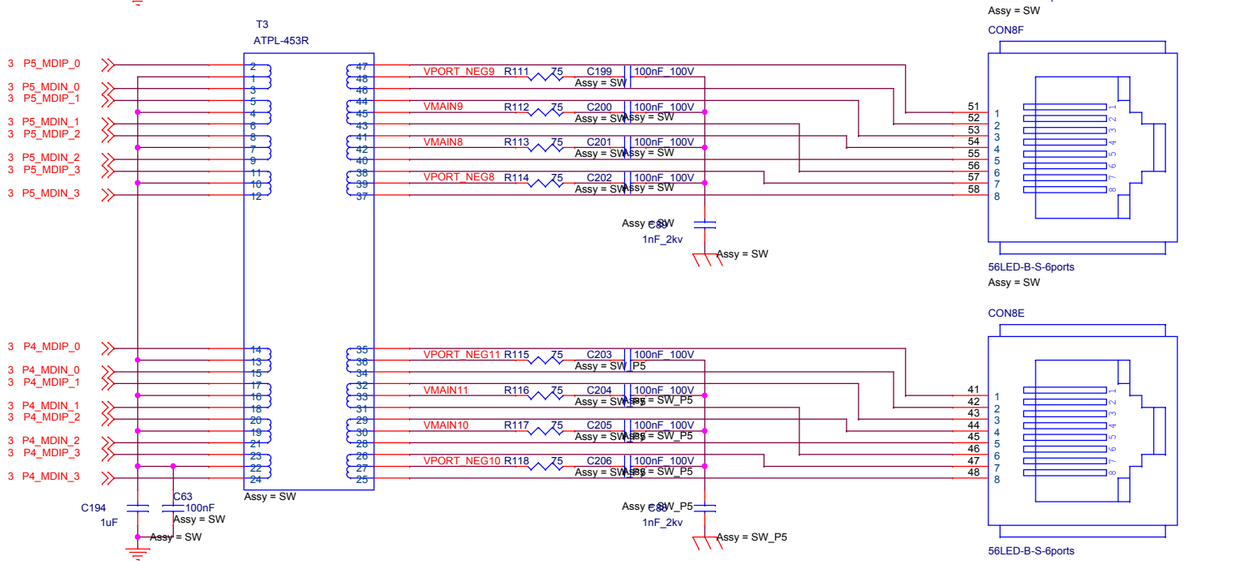
PORT-3 MDI I/F

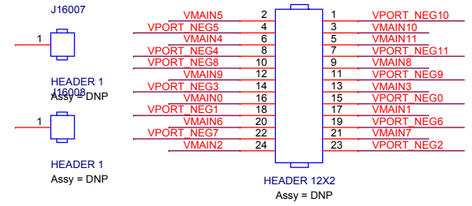


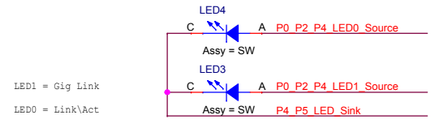
PORT-2 MDI I/F

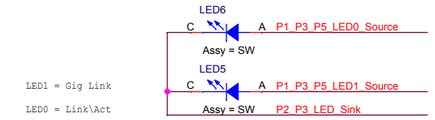


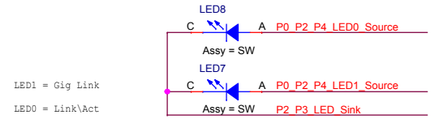
PORT-4 MDI I/F

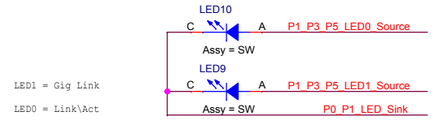


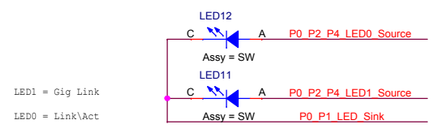


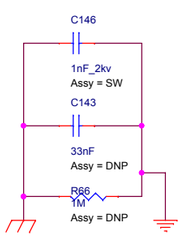


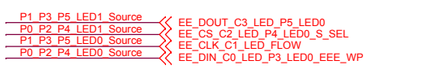












	C0 LED	C1 LED	C2 LED	C3 LED
R0 LED	Port 0 LED 0	Port 1 LED 0	Port 0 LED 1	Port 1 LED 1
R1 LED	Port 2 LED 0	Port 3 LED 0	Port 2 LED 1	Port 3 LED 1
R2 LED	Port 4 LED 0	Port 5 LED 0	Port 4 LED 1	Port 5 LED 1

Size	Title	Rev
C	ClearFog Pro Evaluation Board	Rev-2.1

Date: Wednesday, October 28, 2015 Sheet 19 of 19