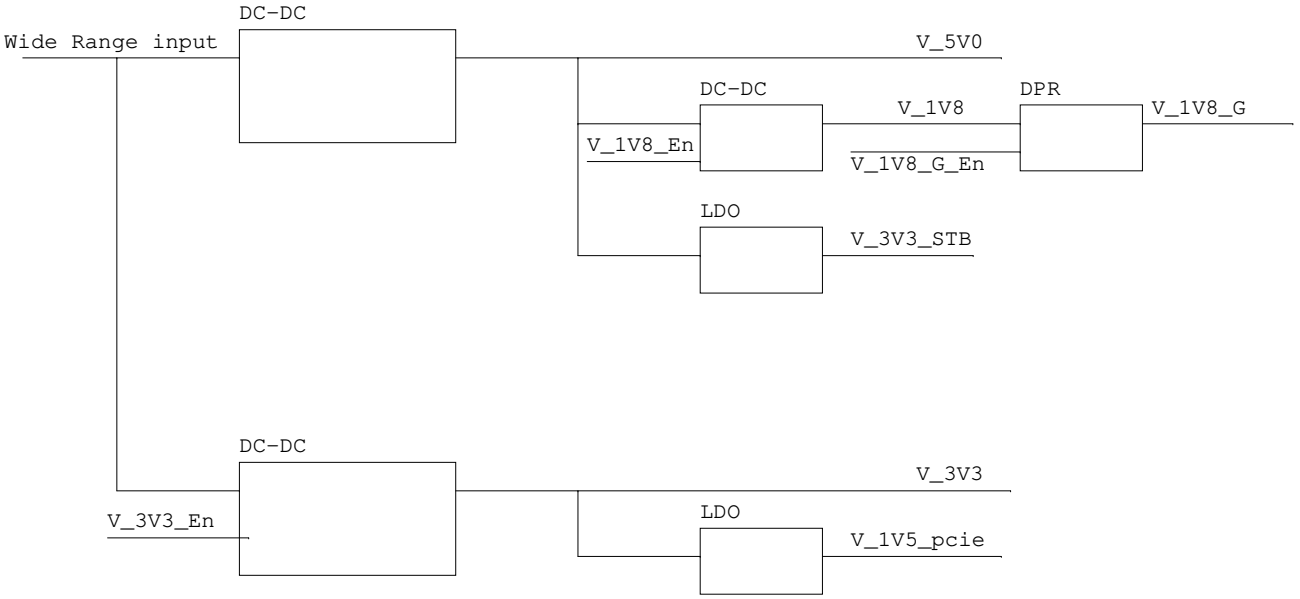
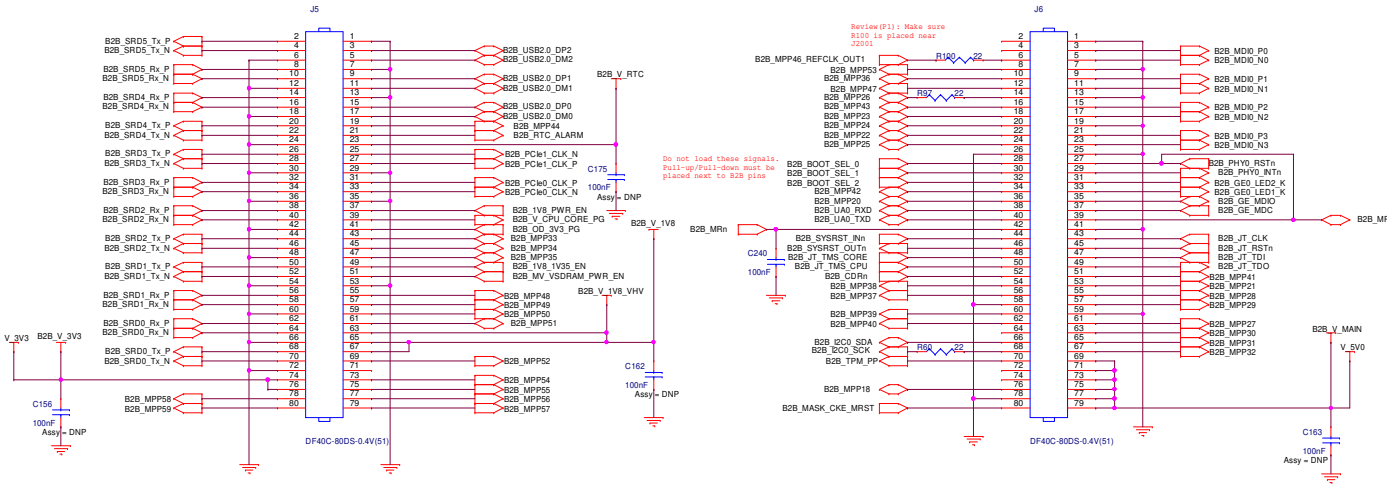
To Extract BOM:
---
Item\tQuantity\tAssemblyOption\tPart\tPCB Footprint\tDescription\tDataSheet\tManufacturer\tManufacturer P/N\tSolidRun P/N\tReference
{Item}\t{Quantity}\t{ASSY}\t{Value}\t{PCB Footprint}\t{DESCRIPTION}\t{Datasheet}\t{Manufacturer}\t{Manufacturer P/N}\t{SolidRun P/N}\t{Reference}



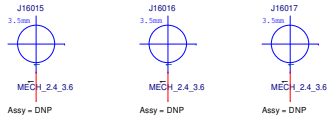



| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, October 28, 2015 Sheet 1 of 19



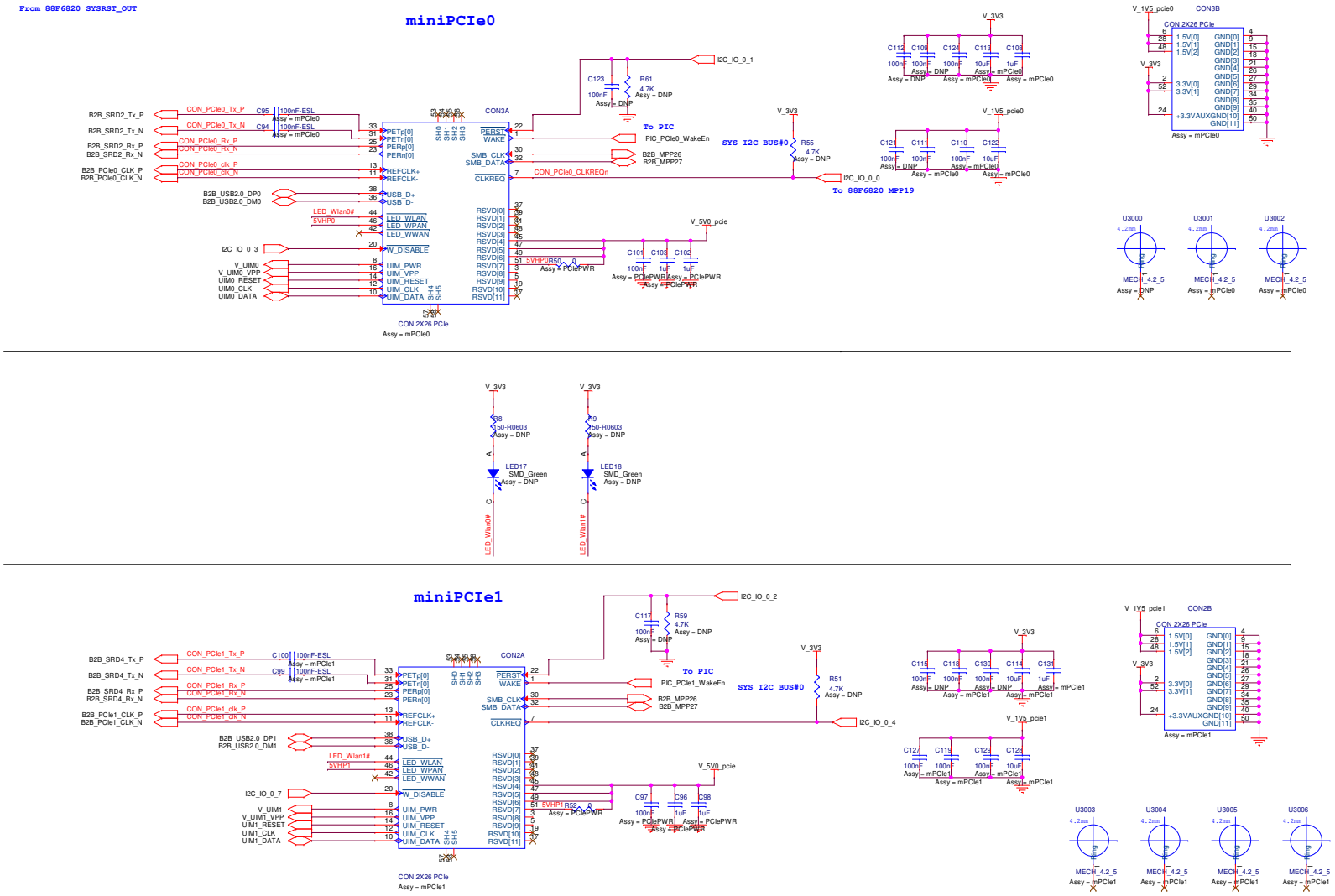

Three mechanical holes for the MicroSoM







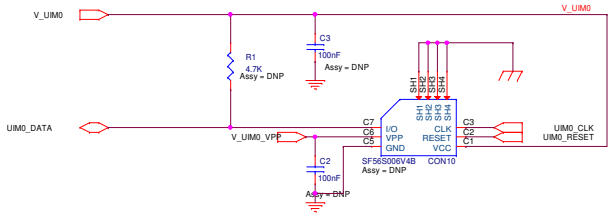
| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |
| Date: Tuesday, June 18, 2019 | Sheet 2 of 19 | |

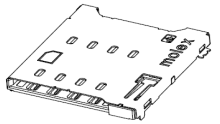





| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |
| Date: Tuesday, June 04, 2019 | Sheet 3 of 19 | |

## uSIM connector
## Push-Push



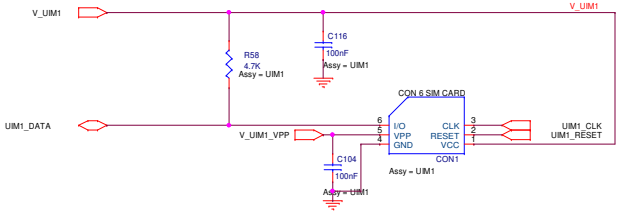
[ SIM CARD PIN-MAP ]

| PIN NO. | DESCRIPTION |
|---|---|
| #1 | Vcc(Supply V) |
| #2 | RST(Reset) |
| #3 | CLK(Clock) |
| #4 | Reserved |
| #5 | GND |
| #6 | Vpp(Program V) |
| #7 | I/O |
| #8 | Reserved |

| | |
|---|---|
| G1~G6 | GND |
| Detect | Card Detector |
| Switch | Common/GND |

| Card Insertion Condition | DETECT SWITCH |
|---|---|
| Without Card | Open (OFF) |
| Card Insertion | Close (ON) |

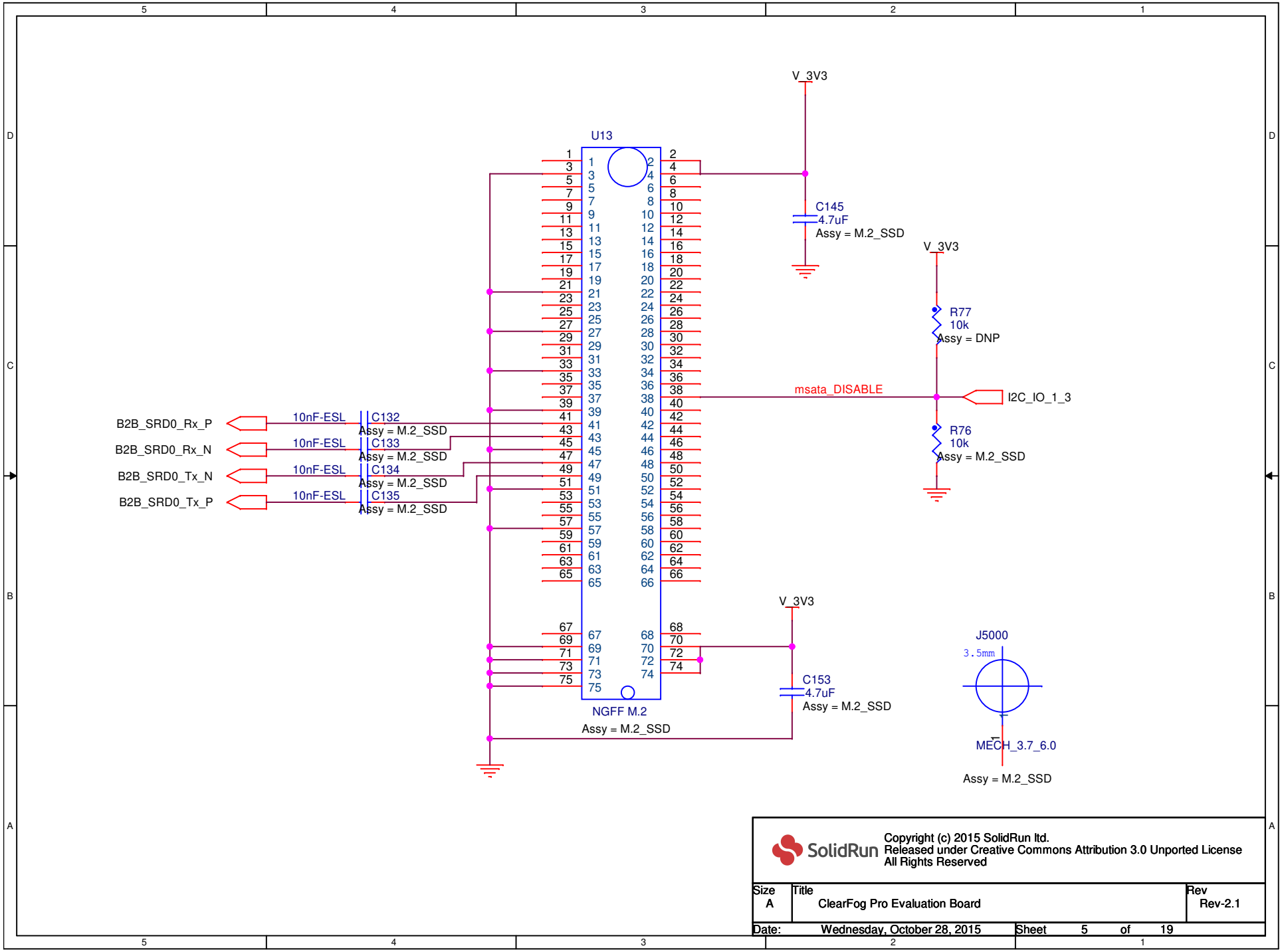
## SIM connector
## Henge






| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, October 28, 2015 Sheet 4 of 19






| Size | Title | Rev |
|---|---|---|
| A | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, October 28, 2015 Sheet 5 of 19

**USB2.0**
**- Common Mode Choke**

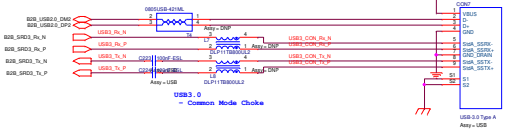
Connector side

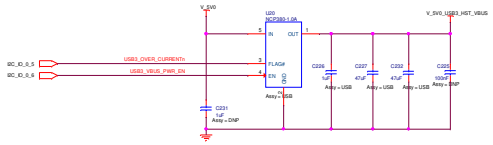
**5v/1A Power out to USB3 device**

V_5V0_USB3_HST_VBUS

**MV USB3.0 HOST**

[TYPE-A]

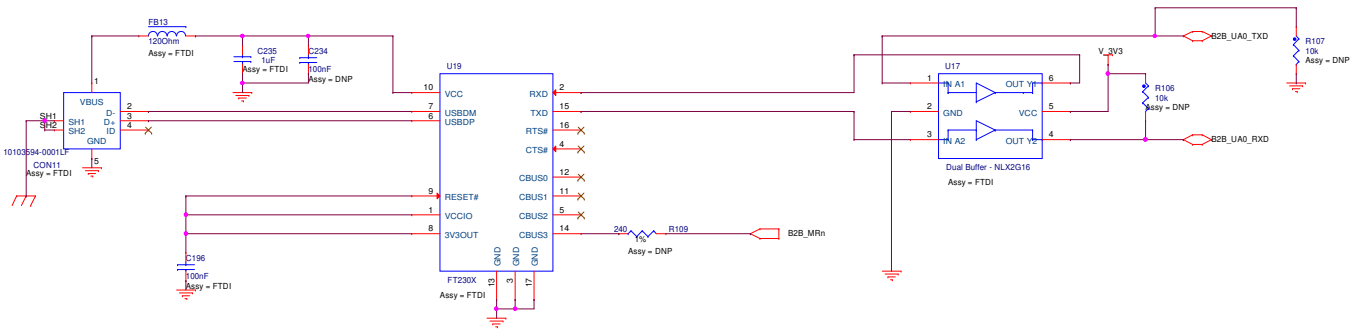





| | | |
|---|---|---|
| Size: D | Title: CloneFog Pro Evaluation Board | Rev: Rev:2.1 |
| Date: Tuesday, June 16, 2015 | Sheet 6 of 19 | |

# microUSB to UART

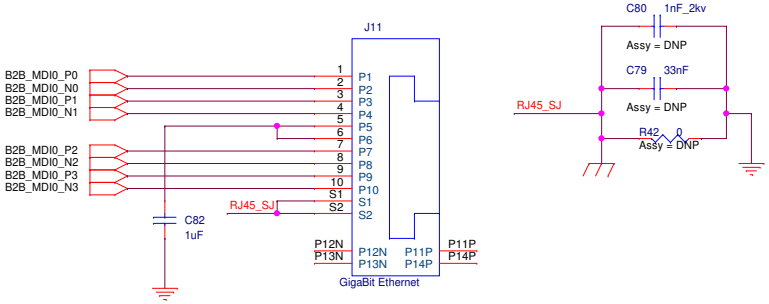


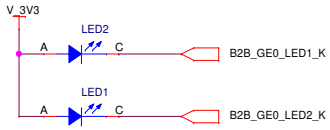



| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, October 28, 2015 Sheet 7 of 19

# GE0: RJ45 Connector



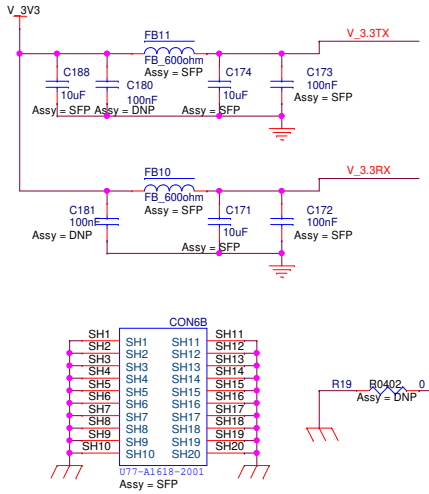



| Size | Title | Rev |
|---|---|---|
| B | ClearFog Pro Evaluation Board | Rev-2.1 |

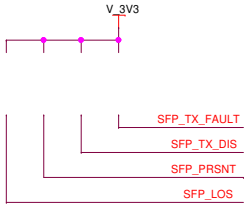
Date: Wednesday, October 28, 2015 Sheet 8 of 19

SFP + defines maximum current withdraw from V_3.3TX and V_3.3RX as 300mA each.

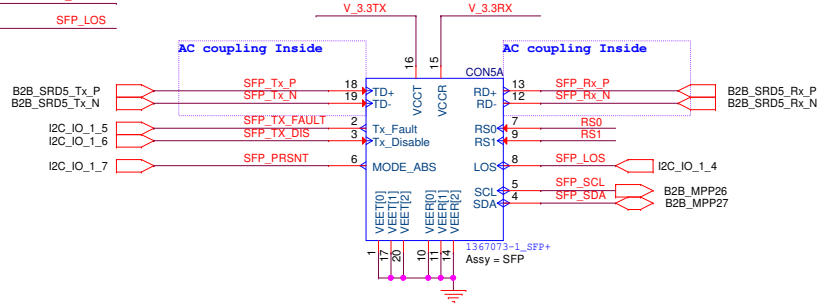
## SFP TRANSCEIVER Power

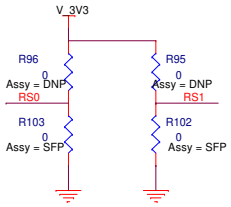



Replaced/Removed pullups with I2C_IO expander's pullups.




## SFP TRANSCEIVER



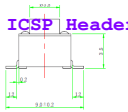





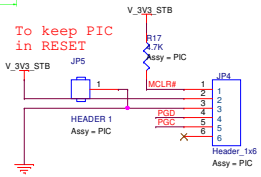

| Size | Title | Rev |
|---|---|---|
| B | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Tuesday, June 04, 2019 Sheet 9 of 19

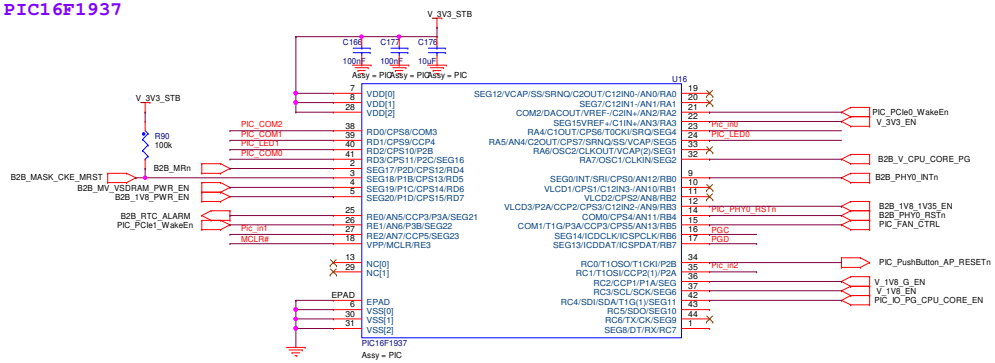
## ICSP Header



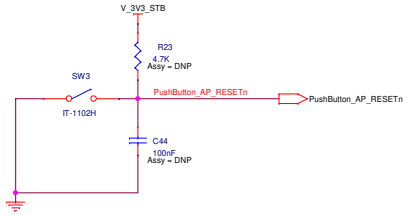
To keep PIC in RESET

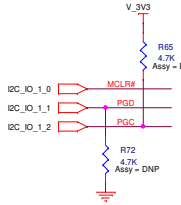



## PIC16F1937

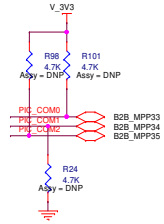



## AP Reset Switch (GPIO)

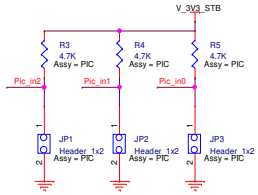


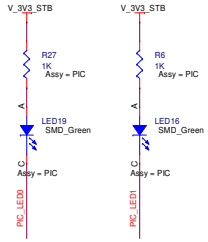

## COM with MV Device




## For SW Configuration Usage




## LEDs

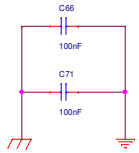




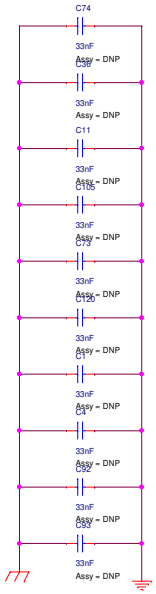

| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Friday, June 10, 2016 Sheet 10 of 19

Bypass capacitors for MDIO
passing underneath GNDC

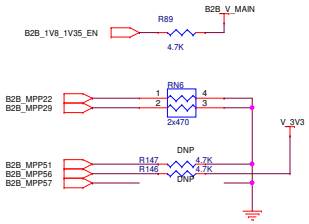


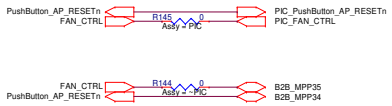

Bypass capacitors between GNDC and GND





Carrier DC-DC PGOOD Signals will enable CPU DC-DC
on uSoM. Signal is pulled up on uSom.

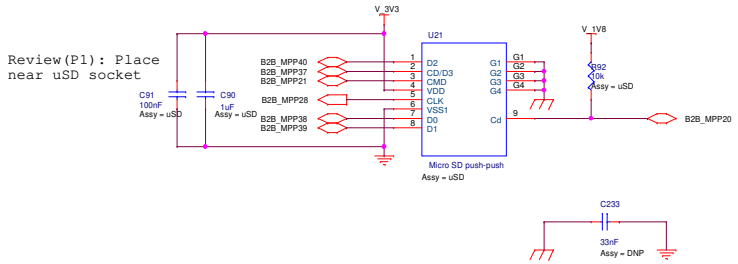






| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

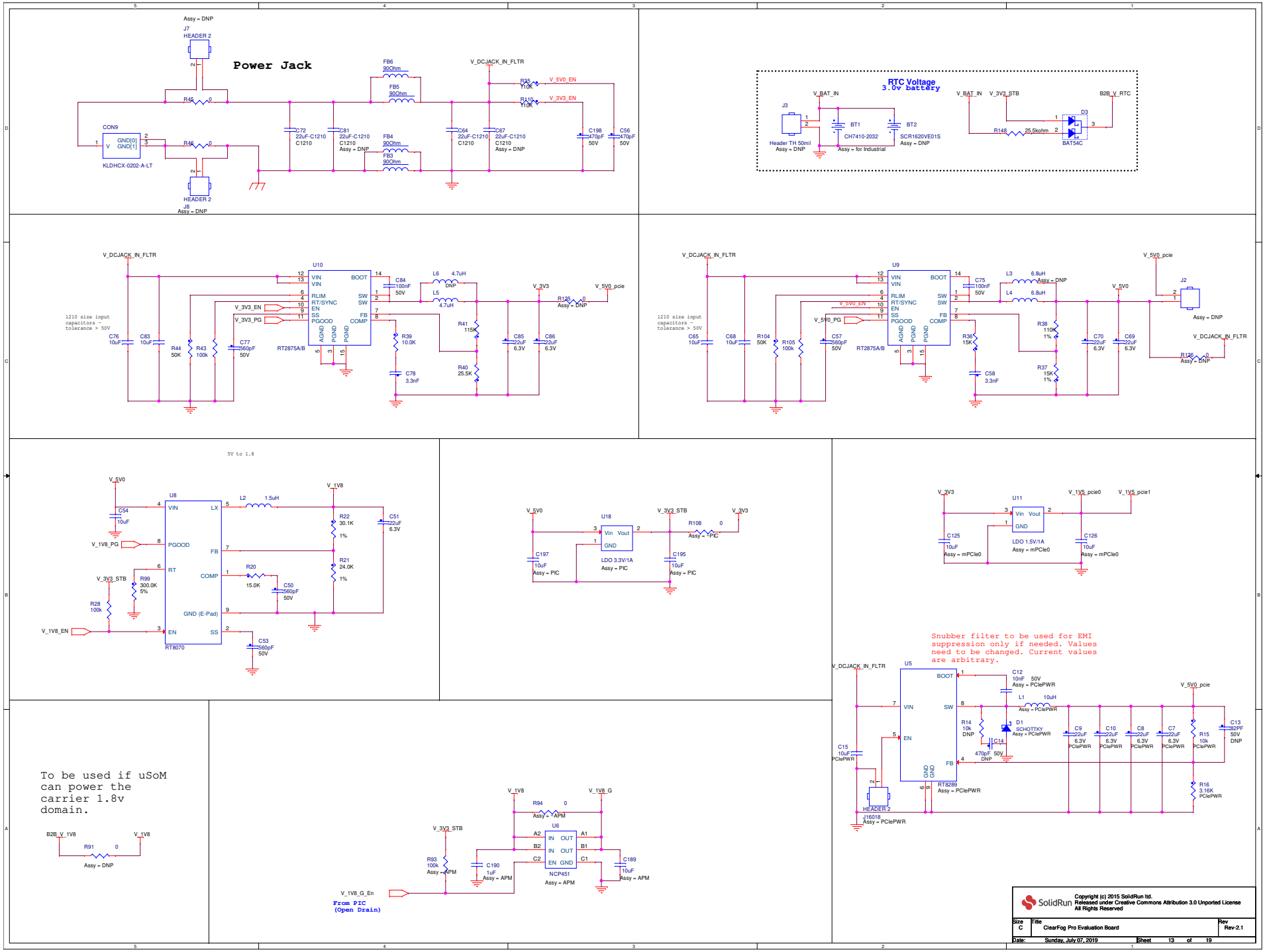
Date: Tuesday, June 18, 2019 Sheet 11 of 19



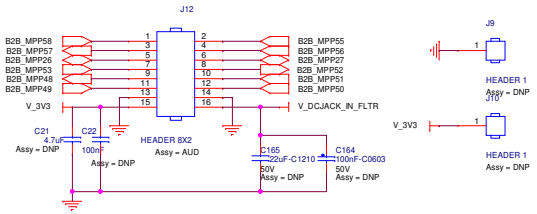


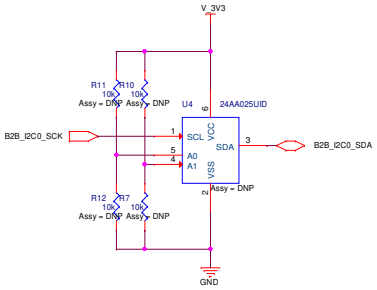

| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

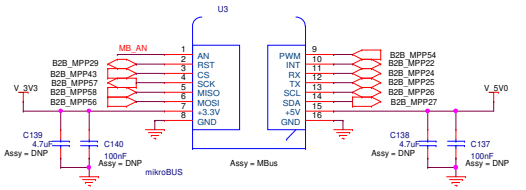
Date: Wednesday, October 28, 2015 Sheet 12 of 19


Power Jack
Assy = DNP
J7
HEADER 2
J8
HEADER 2
CON9
KLDHCX-0202-A-LT
R45
R46
FB6
90Ohm
FB5
90Ohm
FB4
90Ohm
FB3
90Ohm
V_DCJACK_IN_FLTR
R25
110K
R110
110K
V_5V0_EN
V_3V3_EN
C72
22uF-C1210
C1210
C81
22uF-C1210
C1210
Assy = DNP
C64
22uF-C1210
C1210
C67
22uF-C1210
C1210
Assy = DNP
C198
470pF
50V
C56
470pF
50V
RTC Voltage
3.0v battery
V_BAT_IN
J3
Header TH 50mil
Assy = DNP
BT1
CH7410-2032
BT2
SCR1620VE01S
Assy = DNP
Assy = for Industrial
V_BAT_IN
V_3V3_STB
B2B_V_RTC
D3
R148
25.5kohm
BAT54C
V_DCJACK_IN_FLTR
U10
VIN
VIN
RLIM
RT/SYNC
EN
SS
PGOOD
BOOT
SW
SW
FB
COMP
AGND
PGND
PGND
RT2875A/B
V_3V3_EN
V_3V3_PG
1210 size input
capacitors -
tolerance > 50V
C76
10uF
C83
10uF
R44
50K
R43
100k
C77
560pF
50V
C84
100nF
50V
L6
4.7uH
DNP
L5
4.7uH
R39
10.0K
C78
3.3nF
R41
115K
R40
25.5K
C85
22uF
6.3V
C86
22uF
6.3V
V_3V3
R125
0
Assy = DNP
V_5V0_pcie
V_DCJACK_IN_FLTR
U9
VIN
VIN
RLIM
RT/SYNC
EN
SS
PGOOD
BOOT
SW
SW
FB
COMP
AGND
PGND
PGND
RT2875A/B
V_5V0_EN
V_5V0_PG
1210 size input
capacitors -
tolerance > 50V
C65
10uF
C68
10uF
R104
50K
R105
100k
C57
560pF
50V
C75
100nF
50V
L3
6.8uH
Assy = DNP
L4
6.8uH
R36
15K
C58
3.3nF
R38
110K
1%
R37
15K
1%
C70
22uF
6.3V
C69
22uF
6.3V
V_5V0
V_5V0_pcie
J2
Assy = DNP
V_DCJACK_IN_FLTR
R126
0
Assy = DNP
5V to 1.8
V_5V0
U8
VIN
LX
PGOOD
FB
RT
COMP
GND (E-Pad)
EN
SS
RT8070
C54
10uF
L2
1.5uH
V_1V8
R22
30.1K
1%
R21
24.0K
1%
C51
22uF
6.3V
V_1V8_PG
V_3V3_STB
R99
300.0K
5%
R28
100k
R20
15.0K
C50
560pF
50V
V_1V8_EN
C53
560pF
50V
V_5V0
U18
Vin
Vout
GND
LDO 3.3V/1A
Assy = PIC
C197
10uF
Assy = PIC
V_3V3_STB
R108
0
Assy = PIC
C195
10uF
Assy = PIC
V_3V3
V_3V3
U11
Vin
Vout
GND
LDO 1.5V/1A
Assy = mPCIe0
C125
10uF
Assy = mPCIe0
V_1V5_pcie0
V_1V5_pcie1
C126
10uF
Assy = mPCIe0
Snubber filter to be used for EMI
suppression only if needed. Values
need to be changed. Current values
are arbitrary.
V_DCJACK_IN_FLTR
U5
BOOT
VIN
SW
EN
FB
GND
GND
RT8289
Assy = PCIePWR
C12
10uF
50V
Assy = PCIePWR
L1
10uH
Assy = PCIePWR
D1
SCHOTTKY
Assy = PCIePWR
C14
470pF
50V
DNP
R14
10k
DNP
C15
10uF
PCIePWR
HEADER 2
J16018
Assy = PCIePWR
C9
22uF
6.3V
PCIePWR
C10
22uF
6.3V
PCIePWR
C8
22uF
6.3V
PCIePWR
C7
22uF
6.3V
PCIePWR
V_5V0_pcie
R15
10k
PCIePWR
C13
82PF
50V
DNP
R16
3.16K
PCIePWR
To be used if uSoM
can power the
carrier 1.8v
domain.
B2B_V_1V8
R91
0
Assy = DNP
V_1V8
V_1V8_G
R94
0
Assy = APM
V_3V3_STB
R93
100k
Assy = APM
U6
IN
OUT
IN
OUT
EN
GND
NCP451
Assy = APM
C190
1uF
Assy = APM
C189
10uF
Assy = APM
V_1V8_G_En
From PIC
(Open Drain)
SolidRun
Copyright (c) 2015 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved
Size
C
Title
ClearFog Pro Evaluation Board
Rev
Rev-2.1
Date:
Sunday, July 07, 2019
Sheet
13
of
19

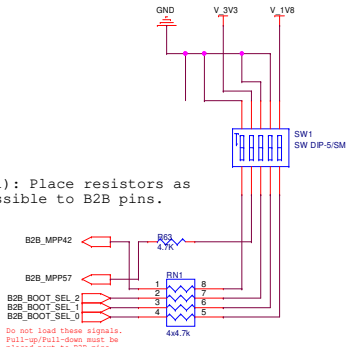
## SLIC TDM Module connectors



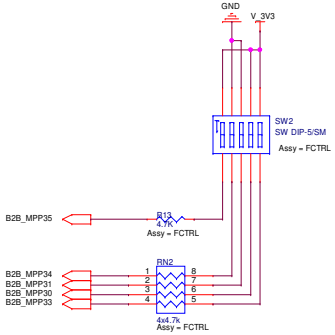




Internally pulled to 0x36:
110110




Internally pulled to 0x0c:
01100




Layout(P1): Place resistors as close possible to B2B pins.

| PART NO. | XX | X | /XX |
|---|---|---|---|
| Device | Address Options | Temperature Range | Package |

Device: MCP3021T: 10-Bit 2-Wire Serial A/D Converter (Tape and Reel)

Temperature Range: E = -40°C to +125°C

Address Options:

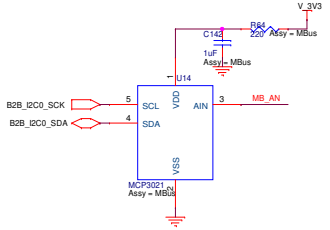
| XX | | A2 | A1 | A0 |
|---|---|---|---|---|
| A0 | = | 0 | 0 | 0 |
| A1 | = | 0 | 0 | 1 |
| A2 | = | 0 | 1 | 0 |
| A3 | = | 0 | 1 | 1 |
| A4 | = | 1 | 0 | 0 |
| A5 * | = | 1 | 0 | 1 |
| A6 | = | 1 | 1 | 0 |
| A7 | = | 1 | 1 | 1 |

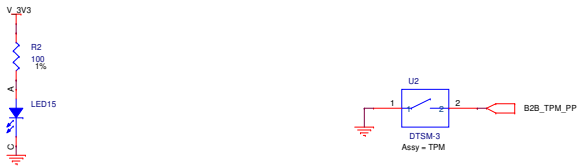
* Default option. Contact Microchip factory for other address options

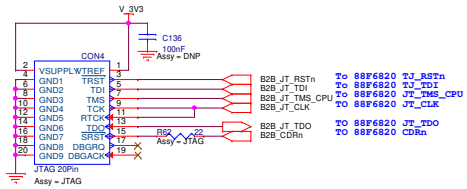
Package: OT = SOT-23, 5-lead (Tape and Reel)

**Examples:**

a) MCP3021A0T-E/OT: Extended, A0 Address, Tape and Reel
b) MCP3021A1T-E/OT: Extended, A1 Address, Tape and Reel
c) MCP3021A2T-E/OT: Extended, A2 Address, Tape and Reel
d) MCP3021A3T-E/OT: Extended, A3 Address, Tape and Reel
e) MCP3021A4T-E/OT: Extended, A4 Address, Tape and Reel
f) MCP3021A5T-E/OT: Extended, A5 Address, Tape and Reel
g) MCP3021A6T-E/OT: Extended, A6 Address, Tape and Reel
h) MCP3021A7T-IE/OT: Extended, A7 Address, Tape and Reel



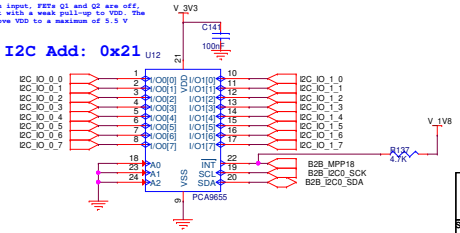

## PCA9555
## 16-bit I2C and SMBus I/O port with interrupt
## 5 V tolerant I/Os

I/O port
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up to VDD. The input voltage may be raised above VDD to a maximum of 5.5 V

### I/O Table

| | |
|---|---|
| IO2_0 | |
| IO2_1 | |
| IO2_2 | |
| IO2_3 | |
| IO2_4 | |
| IO2_5 | |
| IO2_6 | |
| IO2_7 | |
| IO3_0 | |
| IO3_1 | |
| IO3_2 | |
| IO3_3 | |
| IO3_4 | |
| IO3_5 | |
| IO3_6 | |
| IO3_7 | |

### I2C Add: 0x21

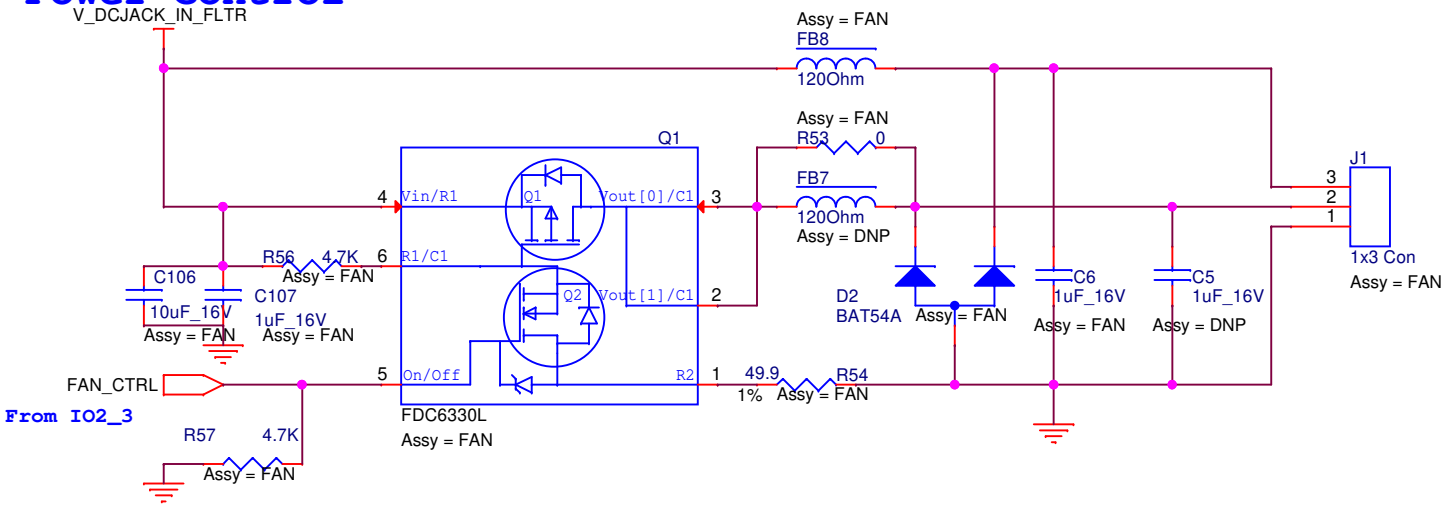





| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, June 19, 2019 Sheet 14 of 19

# FAN Power Control

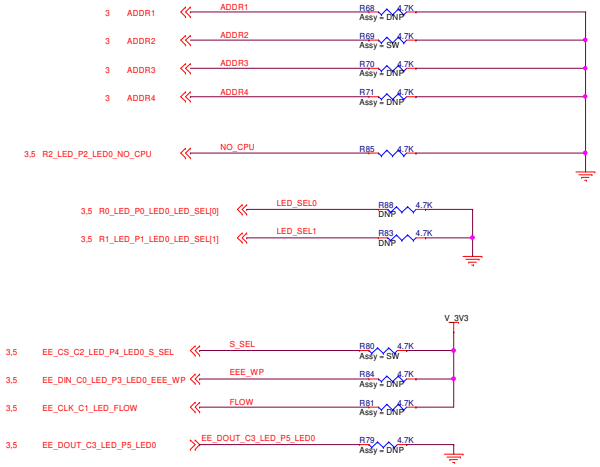





| Size | Title | Rev |
|---|---|---|
| A | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, October 28, 2015 Sheet 15 of 19

**ADDR0 = alway 0x0**
**SMI ADDRESS is the inverted value = 0x4**



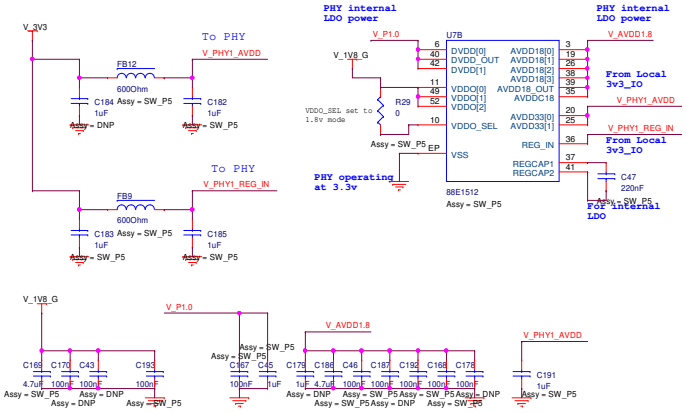
| Pin | Name | Functionality | Default | Jumper/ DPR |
|---|---|---|---|---|
| 35 | NO_CPU | CPU ATTACHED | PU | PD.NC |
| 34 | LED_SEL[1] | LED Functionality | PU | PD.NC |
| 33 | LED_SEL[0] | LED Functionality | PU | PD.NC |
| 39 | S_SEL | Connect serdes to port 4 or 5 | PD | PU |
| 38 | FLOW | Advertise auto-neg flow control | PD | PU |
| 36 | EEE_WP | Enable energy efficient Ethernet | PD | PU.NC |
| 70 | P5_VDDOS[0] | Port 5 power rail select | PU | PD |
| 66 | P5_VDDOS[1] | Port 5 power rail select | PU | PU |
| 67,68,69 | P5_OUTD[2:0] | 0x7 = RGMII | PU | No option |
| 94 | P6_VDDOS[0] | Port 6 power rail select | PU | PD |
| 90 | P6_VDDOS[1] | Port 6 power rail select | PU | PU |
| 91,92,93 | P6_OUTD[2:0] | 0x7 = RGMII | PU | No option |
| 85,86,87,88 | ADDR[4:1]n | SMI ADDRESS | PU | 0x2 |



Size C | Title ClearFog Pro Evaluation Board | Rev Rev-2.1
Date: Tuesday, June 04, 2019 | Sheet 16 of 19

## PHY Power configurations

**88E1512 power configurations:**
**1. using internal 1v8 and 1v0 regulators.**
**2. VDDO_SEL configs VDDO to operate at 2v5/3v3.**




## PHYADD configuration

**88E1512 PHY configuration options:**
**PHY_address=1**

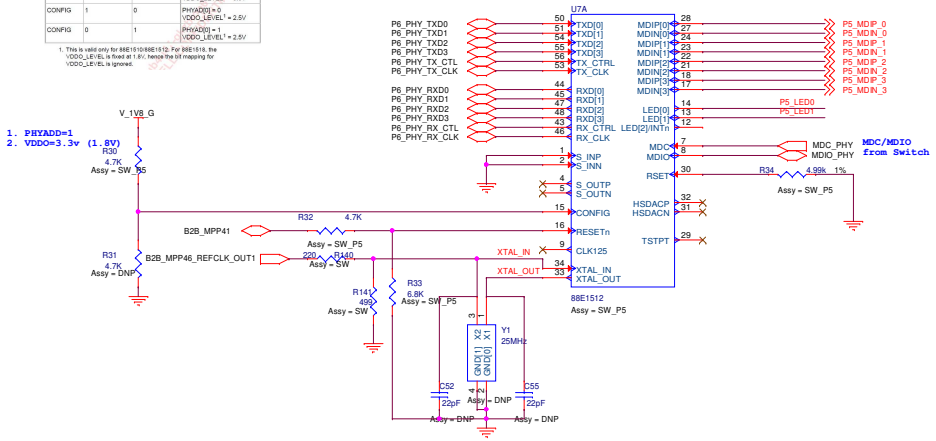
Table 53: Configuration Mapping

| Pin | CONFIG Bit1 | CONFIG Bit 0 | Value Assignment |
|---|---|---|---|
| CONFIG | 0 | 0 | PHYAD[0] = 0<br>VDDO_LEVEL[1] = 3.3V |
| CONFIG | 1 | 1 | PHYAD[0] = 1<br>VDDO_LEVEL[1] = 3.3V |
| CONFIG | 1 | 0 | PHYAD[0] = 0<br>VDDO_LEVEL[1] = 2.5V |
| CONFIG | 0 | 1 | PHYAD[0] = 1<br>VDDO_LEVEL[1] = 2.5V |

1. This is valid only for 88E1510/88E1512. For 88E1518, the VDDO_LEVEL is fixed at 1.8V, hence the bit mapping for VDDO_LEVEL is ignored.

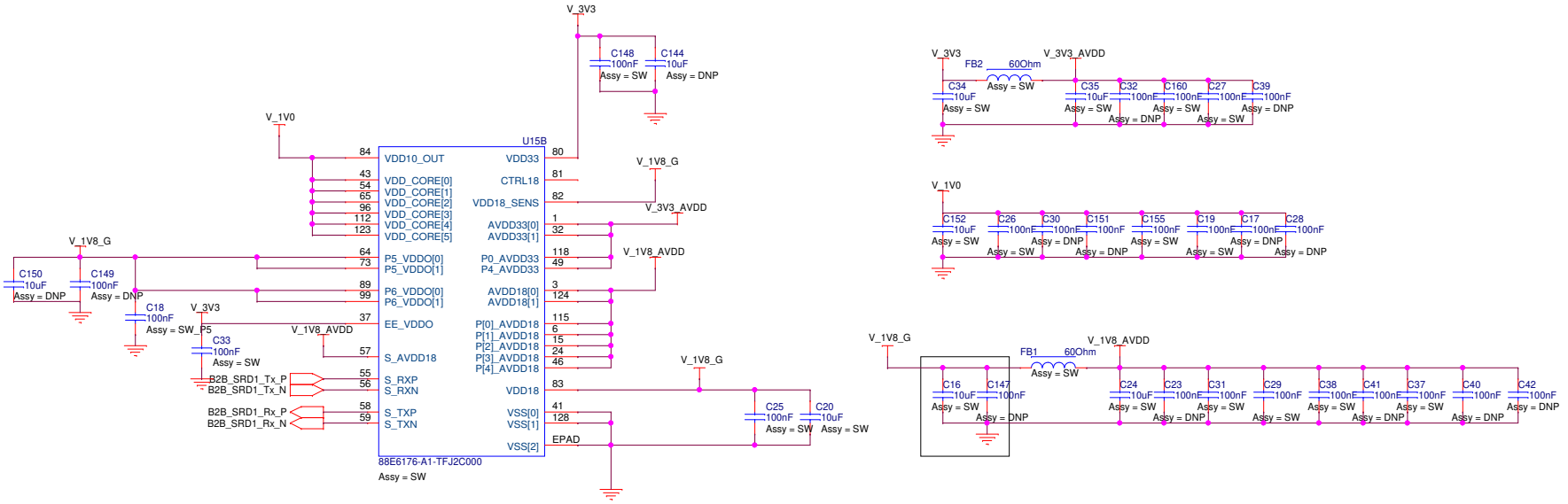


**1. PHYADD=1**
**2. VDDO=3.3v (1.8V)**





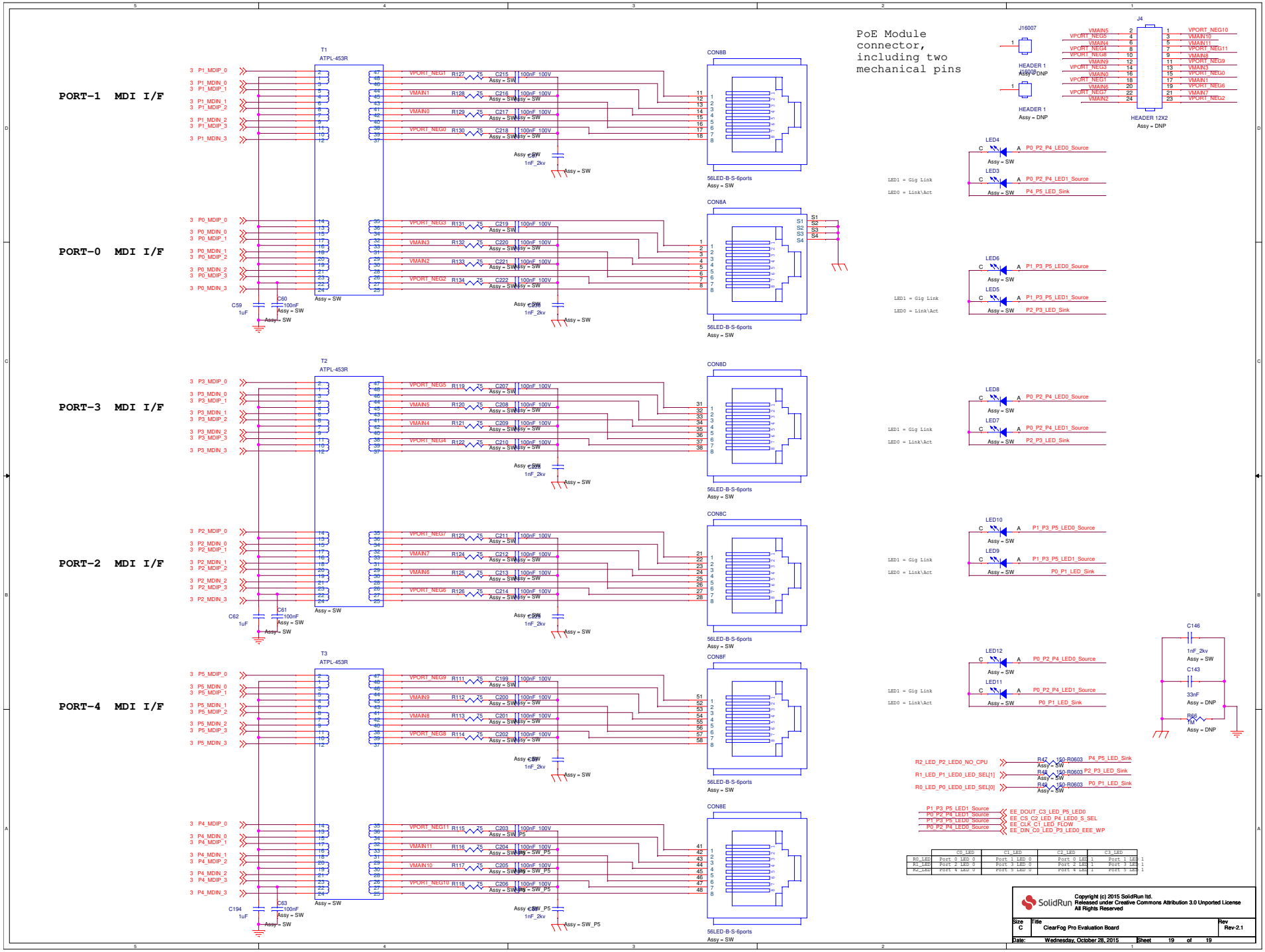

| Size | Title | Rev |
|---|---|---|
| C | ClearFog Pro Evaluation Board | Rev-2.1 |
| Date: Sunday, February 12, 2017 | Sheet 17 of 19 | |






| Size | Title | Rev |
|---|---|---|
| B | ClearFog Pro Evaluation Board | Rev-2.1 |

Date: Wednesday, October 28, 2015 Sheet 18 of 19


PoE Module connector, including two mechanical pins
PORT-1 MDI I/F
PORT-0 MDI I/F
PORT-3 MDI I/F
PORT-2 MDI I/F
PORT-4 MDI I/F
T1
T2
T3
ATPL-453R
CON8B
CON8A
CON8D
CON8C
CON8F
CON8E
56LED-B-S-6ports
J16007
HEADER 1
Assy = DNP
J4
HEADER 12X2
LED4
LED3
LED6
LED5
LED8
LED7
LED10
LED9
LED12
LED11
LED1 = Gig Link
LED0 = Link\Act
C146
1nF_2kv
C143
33nF
R66
1M
R2_LED_P2_LED0_NO_CPU
R1_LED_P1_LED0_LED_SEL[1]
R0_LED_P0_LED0_LED_SEL[0]
150-R0603
EE_DOUT_C3_LED_P5_LED0
EE_CS_C2_LED_P4_LED0_S_SEL
EE_CLK_C1_LED_FLOW
EE_DIN_C0_LED_P3_LED0_EEE_WP
C0_LED
C1_LED
C2_LED
C3_LED
R0_LED
R1_LED
R2_LED
Copyright (c) 2015 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved
SolidRun
Size C
Title ClearFog Pro Evaluation Board
Rev Rev-2.1
Date: Wednesday, October 28, 2015
Sheet 19 of 19